

MODULE - 2 : BJT Biasing

(1)

Syllabus: BJT Biasing: DC load line & Bias Point, Base bias, voltage divider bias. Numerical examples as applicable

* Transistor biasing (1) Biasing the transistor:

The process of applying external dc voltage to a transistor is called transistor biasing (2) biasing the transistor

(1)

The process of applying external dc voltage to a transistor to operate it in the desired region is called transistor biasing

(2)

The process of applying external dc voltage to a transistor to establish the required dc current and voltage so that it operates in the appropriate region of the characteristic is called transistor biasing

(3)

The proper flow of zero signal collector current & the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing

Note:

(1) For transistor to be an amplifier: It must be operated in the active region of its characteristic (ie for CB configuration, base-emitter junction should be forward biased & collector-base junction should be reverse biased)

(2) For transistor to be a switch: It is operated in the cut-off region (open switch) and/or saturation-region (closed switch).

③ The circuit which provides transistor biasing is known as biasing circuit.

④ The basic conditions for faithful amplification (Conditions for proper biasing of a transistor)

- ① Proper zero signal collector current.
- ② Minimum proper base-emitter Voltage (V_{BE}) at any instant. ($0.3V$ for Ge & $0.7V$ for Si)
- ③ Minimum proper collector-emitter Voltage (V_{CE}) at any instant. ($0.5V$ for Ge & $1V$ for Si)

⑤ Need for biasing:

- ① To turn on the device
- ② To set a fixed level of current & fixed voltage drop across the transistor junctions.
- ③ To operate transistor in the desired region (Since it operates linearly & provides a constant voltage gain)

⑥ Inherent variations of transistor parameters:

In practice, the transistor parameters such as B , V_{BE} are not same for every transistor even of the same type. Ex: For BC147 (Silicon NPN transistor), B varies from 100 to 600 (for one transistor it may be 100, for the other it may be 600).

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. Therefore, the biasing network(circuit) is designed such that it should be able to work with all transistors of one type. In other words, the operating point should be independent of transistor parameters variations.

⑦ Stabilization:

The process of making operating point independent of temperature changes & variations in transistor parameters is known as Stabilization.

⑧ Need for stabilization: ⑨ Factors affecting stability of Q-point:

Stabilization of the operating point @ Q-point is necessary due to the following reasons:

⑩ Temperature dependence of I_C :

- The collector leakage current (I_{C0}) is greatly influenced (especially in Ge transistor) by temperature changes.

⑪ Inherent variations of transistor parameters:

The values of B & V_{BE} are not same for any two transistors even of the same type. Also V_{BE} decreases with increase in temperature.

⑫ Thermal runaway:

The self-destruction of an unstabilized transistor is known as thermal runaway.

The collector leakage current I_{C0} is strongly dependent on temperature.

Higher stability indicates poor
stability, lower = better stability

⑬ Stability factor:

The rate of change of collector current (I_C) w.r.t the device saturation current (I_{C0} @ I_0) at constant B & I_0 is called Stability factor (S)

$$\text{i.e. } S = \frac{dI_C}{dI_{C0}} \text{ at constant } I_B \text{ & } B \quad - (*)$$

K DC Load line and Bias Point :

DC Load line :

Defn: A straight line drawn on the transistor output characteristic is called DC Load line for a transistor circuit. ①

The Load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector resistance (R_C) and a given supply voltage (V_{CC}) [For a common emitter circuit]

② A straight line which shows all corresponding levels of I_C and V_{CE} that can exist in a particular circuit is called DC load line [For CE circuit]

Analyisis:

Consider a n-p-n CE transistor as shown in fig ①

Here supply voltage (V_{CC}) forward biases the base-emitter junction & reverse biases the collector-emitter junction.

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad \text{--- (1)}$$

Case(i): Let $I_C = 0$

Eqn(1) becomes,

$$V_{CE} = V_{CC} \quad \text{--- (2)}$$

Mark point A at

$A(V_{CE}, I_C) = A(0, V_{CC})$
(Transistor in cut-off)

Case(ii): Let $V_{CE} = 0$

Eqn(1) becomes

$$I_C = \frac{V_{CC}}{R_C} \quad \text{--- (3)}$$

Mark point B at

$B(V_{CE}, I_C) = B(0, \frac{V_{CC}}{R_C})$

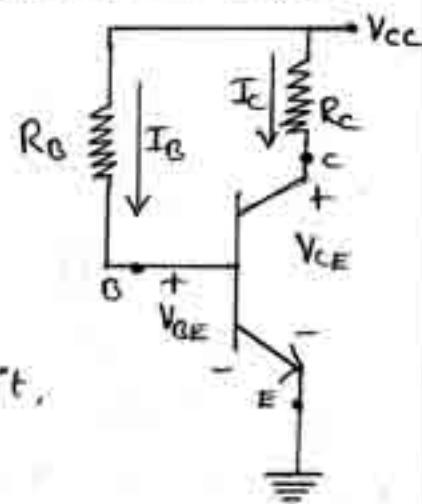
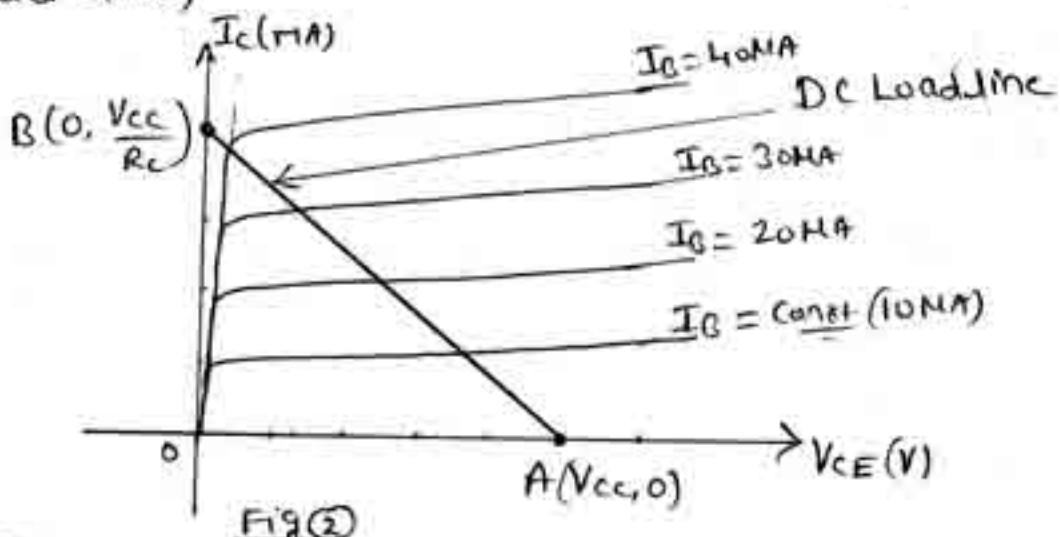


Fig ①: n-p-n CE transistor

(Transistor in saturation)

NOW draw the Straight line through Points A & B
(DC load line)



Fig(2)

Note:

Consider case ①

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow I_C = \left(\frac{-1}{R_C}\right) V_{CE} + \left(\frac{V_{CC}}{R_C}\right) \quad \textcircled{4} \quad \frac{V_{CE}}{(V_{CC})} + \frac{I_C}{(V_{CC}/R_C)} = 1 \quad \textcircled{5}$$

Comparing ④ with $y = mx + c$, we get

$$m = -\frac{1}{R_C} \quad (\text{Slope})$$

Comparing ⑤ with,

$$\frac{x}{a} + \frac{y}{b} = 1, \text{ we get}$$

$$a = V_{CC}, \quad b = V_{CC}/R_C$$

x-intercept (y-intercept)

DC bias Point @ operating Point @ Quiescent Point @ Q-Point @ Silent Point

Defn: The point at which the dc load line intersects with the output characteristic of the transistor & it defines the dc conditions in the circuit is called dc bias Point.

⑥

The point which identifies the transistor collector

(6)

current & collector-emitter voltage when there is no input signal at the base terminal is called dc bias point. ①

A point on the DC load line which represents the zero signal values of V_{CE} (V_{CEQ}) & I_C (I_{CQ}) in a transistor is called dc operating point ② (Q-point).

Analytic:

Consider a n-p-n CE transistor as shown in fig ③

Step ①: Applying KVL to base loop.

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad -⑥$$

$$\Rightarrow I_B = I_{BQ} + \frac{V_{CC} - V_{BE}}{R_B} \quad -⑦$$

Step ②:

$$\text{We have } I_C = I_{CQ} = \beta I_B \quad -⑧$$

Step ③:

Applying KVL to Collector loop.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_C \quad -⑨$$

Step ④:

Now mark Q-point on $Q(V_{CEQ}, I_{CQ})$

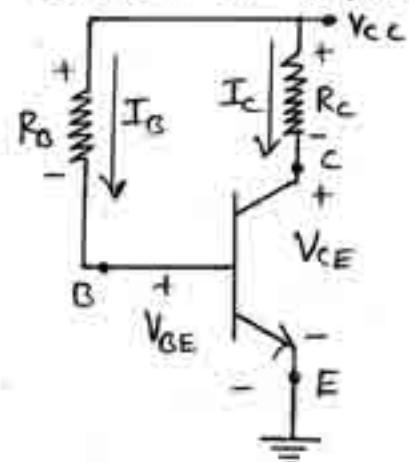
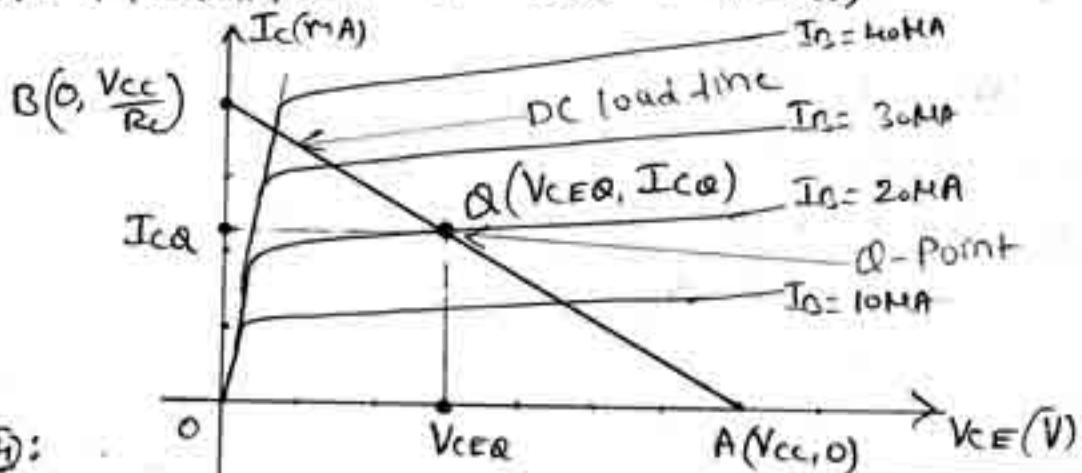


Fig ③: n-p-n CE transistor

Fig ④:

Note:

- ① Consider dc load line drawn on CE output characteristic as shown in fig(5)

→ Here Q_1 is near cut-off region, Q_5 is near saturation region & Q_3 is in the middle of the active region.

→ Selection of Q-point depend on the application of the transistor.

- ② Variation of I_B , I_C & V_{CE} :

→ Here $A(V_{CE}, I_C) = A(20V, 0mA)$

$$B(V_{CE}, I_C) = B(0, 2mA)$$

→ Let us choose Q-point as shown in fig(7).

Now from fig(8).

$$I_B = 20mA$$

$$I_C = 1mA$$

$$V_{CE} = V_{CC} - I_C R_C \\ = 20 - 1 \times 10^3 \times 10 \times 10^{-3} \\ = 10V$$

⇒ At $I_B = 20mA$, $\text{Q}(10V, 1mA)$

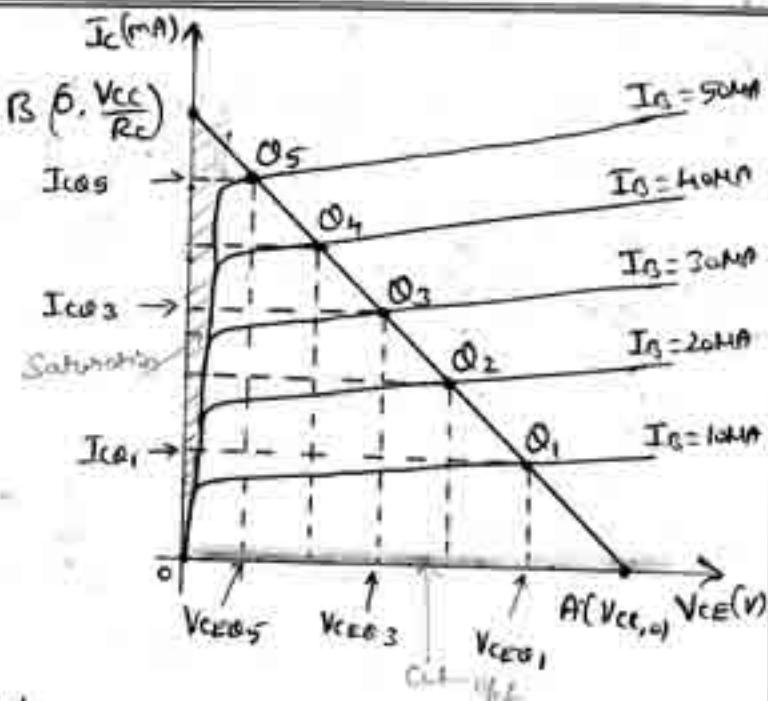
→ When I_B is increased

From $20mA$ to $40mA$,

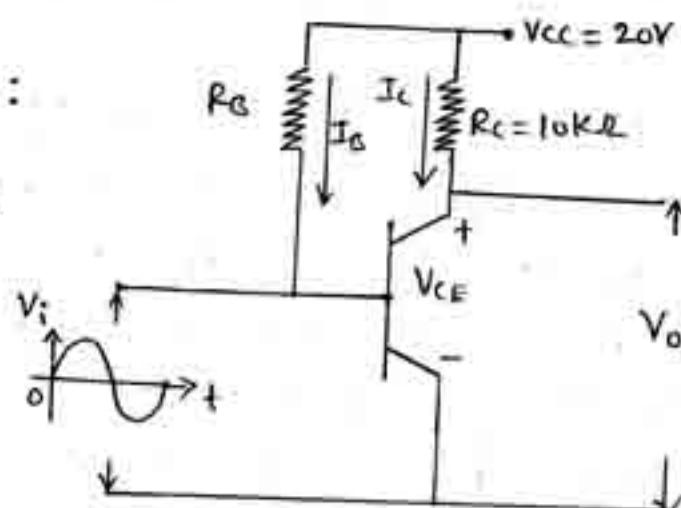
I_C increases from $1mA$ to $1.95mA$

$$1.95mA \approx$$

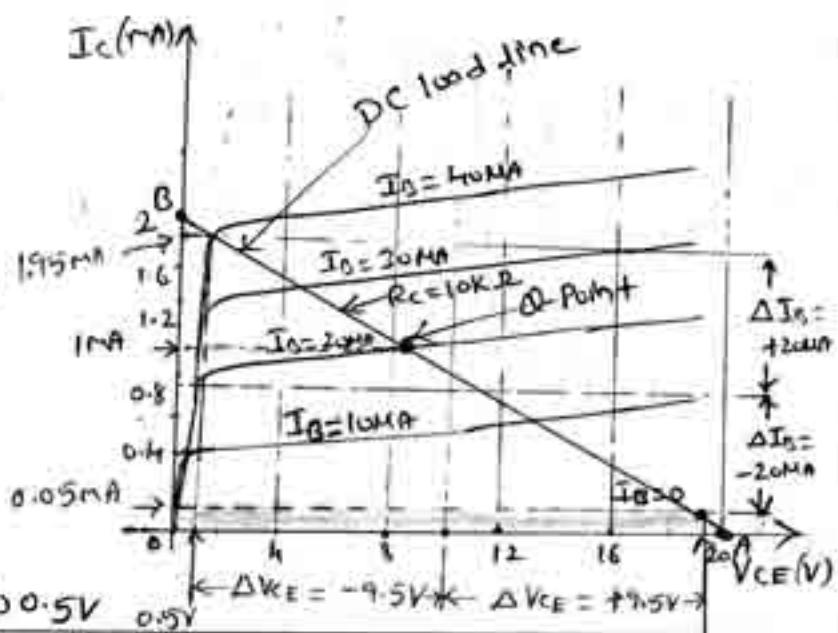
V_{CE} decreases from $10V$ to $0.5V$



Fig(5): CE output characteristics



Fig(6): CE n-p-n transistor



Fig(7):

→ When I_B is decreased from 20mA to 0

I_C decreases from 1mA to 0.05mA &

V_{CE} increases from 10V to 19.5V

∴ By varying input (V_i), I_B , I_C & V_{CE} can be varied

③ Selection of Q-Point: (For CE Configuration)

Based on the application of the transistor, it can be operated in any of the three regions such as

- Saturation @ near Saturation region.
- Cut off region @ near Cut off region.
- Active region @ at the centre of the active region.
- at the centre of the load line.

Fig ⑧ shows the Input Signal applied to base terminal.

④ Near Saturation region (Fig 9):

If Q-Point is located near the Saturation region, the transistor is driven into saturation. Therefore the negative peak of the output voltage (positive peak of the output current) is clipped off. Here we get a distorted output.

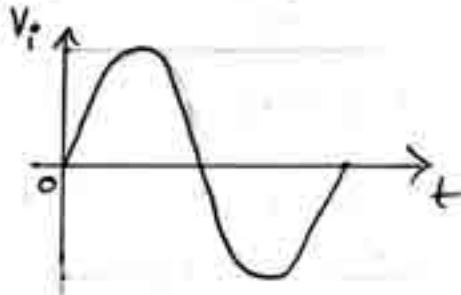


Fig ⑧: INPUT signal

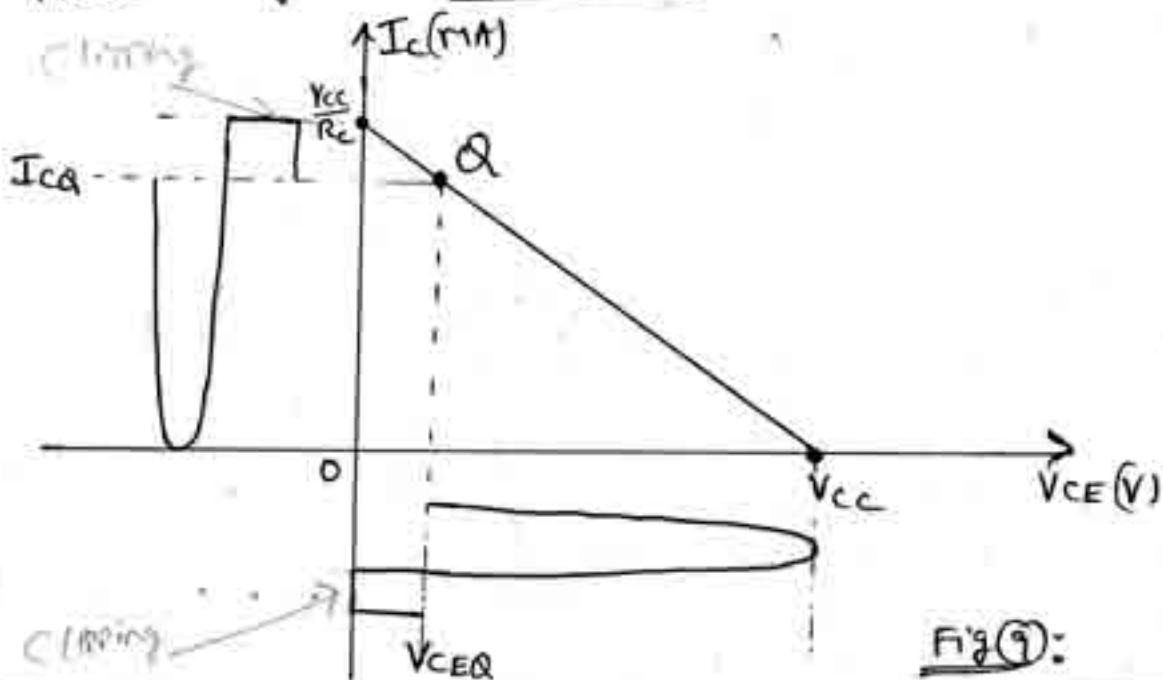


Fig ⑨:

⑥ Near cut-off region (Fig 10)

If Q-point is located near the cut-off region, the transistor is driven into cut-off. Therefore the positive peak of the output voltage (negative peak of the output current) is clipped off. Here we get a distorted output.

⑦ At the centre of the active region (Fig 11)

If Q-point is located at the centre of the load line (active region), the transistor is driven into active region. Here we get an undistorted output.

Conclusion:

For a maximum undistorted output, the transistor should be driven into active region [⑦ Q-point must be located at the centre of the active region (load line)]

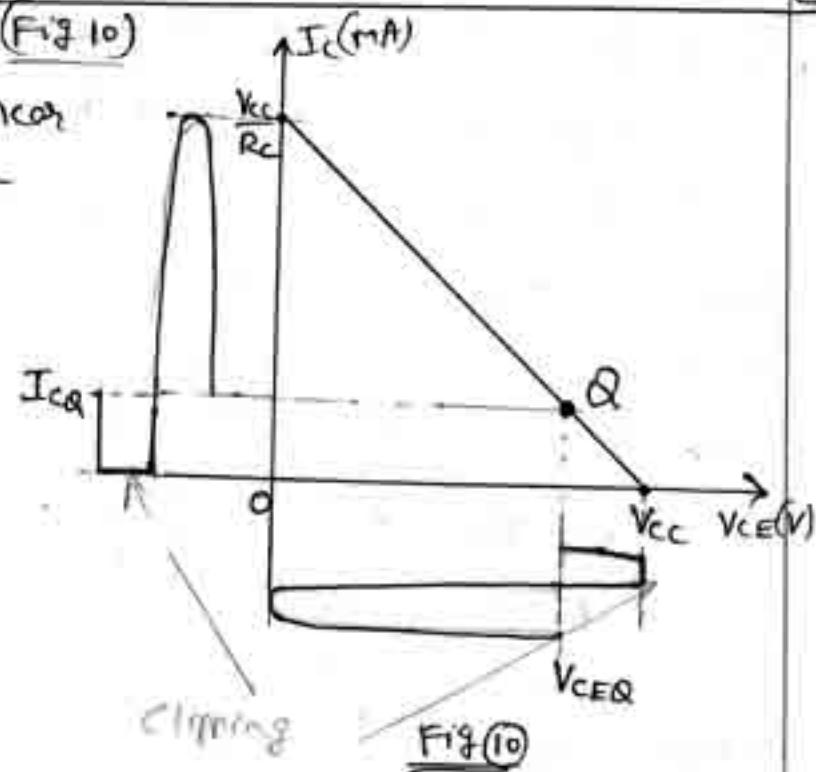


Fig 10

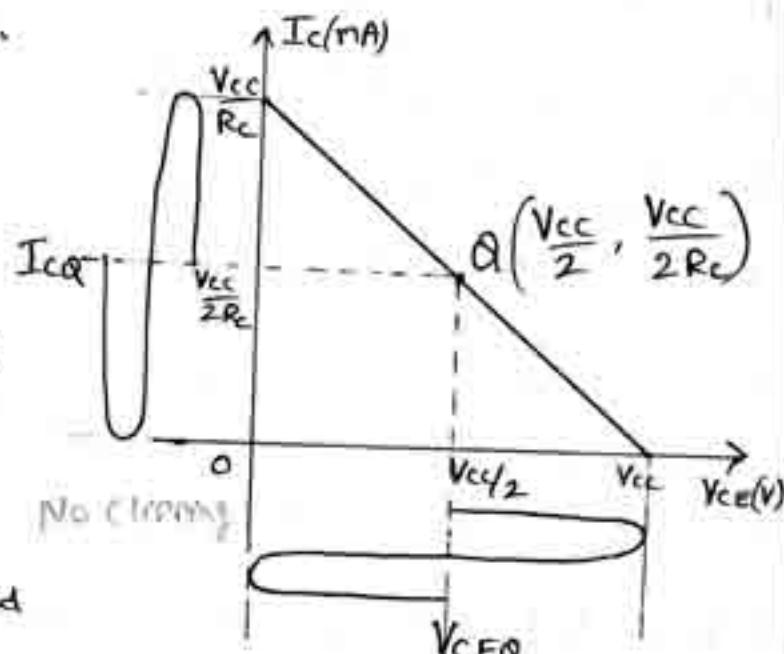


Fig 11

4.

- For large-signal amplification, Q-point must be at the centre of the load line (output voltage swing = $\pm 10V$)
- For small-signal amplification, Q-point need not to be at the centre of the dc load line (output voltage swing not greater than $\pm 1V$)

⑤ Effect of Emitter resistor :

Consider a circuit that has a resistor R_E as shown in fig 12

APPLYING KVL to collector-emitter loop,

$$V_{CC} - V_{CE} - I_C R_E = 0 \quad (\because I_C \approx I_E) \quad -\text{10}$$

CASE(I) Put $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_E} \quad -\text{11}$$

MARK at Point

$$A(V_E, I_C) = (0, \frac{V_{CC}}{R_E})$$

CASE(II) Put $I_C = 0$

$$V_{CE} = V_{CC} \quad -\text{12}$$

Mark at Point

$$B(V_E, I_C) = (V_{CC}, 0)$$

DRAW a straight line through

$$A(0, \frac{V_{CC}}{R_E}) \& B(V_{CC}, 0) \text{ to get}$$

dc load line (shown in fig 14)

Now consider a circuit that has collector & emitter resistors R_C & R_E as shown in fig 13.

APPLYING KVL to collector-emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0 \quad (\because I_C \approx I_E) \quad -\text{13}$$

CASE(I) Put $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C + R_E} \quad -\text{14}$$

Mark at Point

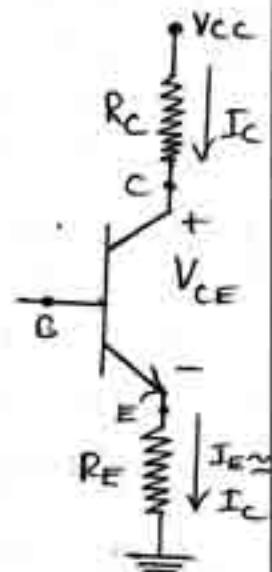
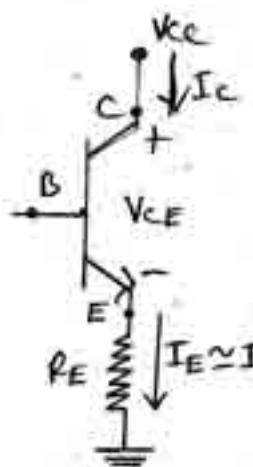
$$A(0, \frac{V_{CC}}{R_C + R_E})$$

CASE(II) Put $I_C = 0$

$$V_{CE} = V_{CC} \quad -\text{15}$$

Mark at Point

$$B(V_{CC}, 0)$$



$$R_L(\text{dc}) = R_E$$

Fig 12

$$R_L(\text{dc}) = R_C + R_E$$

Fig 13

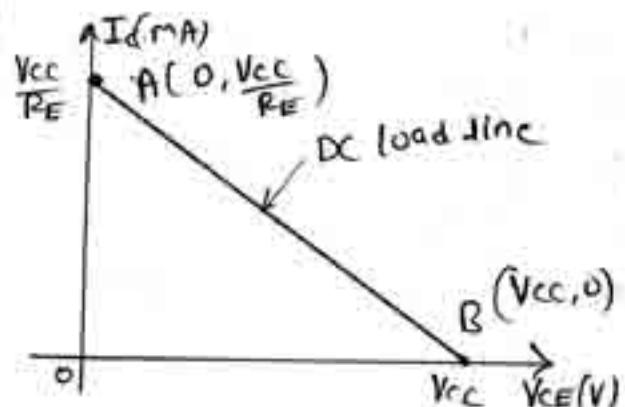


Fig 14:

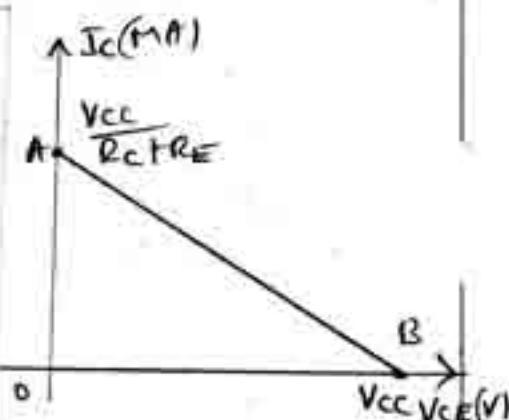


Fig 15:

DRAW a straight line through A & B to get dc load line
(fig 15)

* Methods of transistor biasing:

The most commonly used methods for biasing the transistors are

- ① Base bias ② Fixed bias ③ Fixed Current bias ④ Base resistor bias
- ⑤ Emitter bias ⑥ Emitter feedback bias ⑦ Base bias with emitter feedback.
- ⑧ Collector-to-base bias ⑨ Collector feedback bias.
- ⑩ Base bias with collector feedback.
- ⑪ Voltage-divider bias ⑫ Self bias ⑬ Unbiased bias ⑭ Emitter current bias.

- ① Base bias ② Fixed bias ③ Fixed Current bias ④ Base Resistor bias
- The circuit in which the base current is a constant quantity determined by supply voltage V_{CC} & base resistor R_B (constant quantities) is called fixed bias.

Fig 16 shows the base bias circuit.

Step ①:

APPLYING KVL to base-emitter circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{--- (16)}$$

Step ②:

We have,

$$I_C = h_{FE} I_B \quad \text{--- (17)}$$

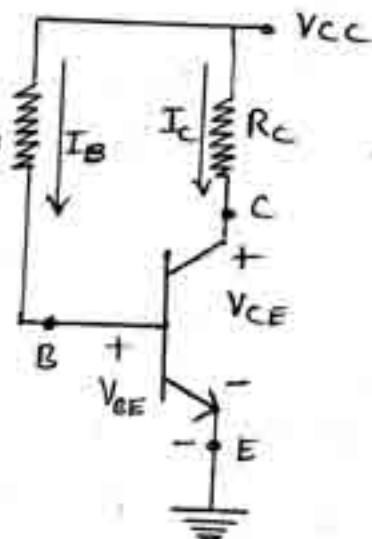


Fig 16: Base bias circuit

Step ③:

APPLYING KVL to collector-emitter circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C \quad \text{--- (18)}$$

When V_{CC} , R_C , R_B & h_{FE} are known, the values of I_B , I_C & V_{CE} can be determined using (16), (17) & (18).

Note:

- ① Effect of $hFE(\text{max}) \ll hFE(\text{min})$: For base bias & voltage divider
When $hFE(\beta)$ is known, the circuit bias conditions (I_B, I_C & V_{CE}) can be determined exactly.

In practice the precise (exact) value of hFE is not known. Therefore the maximum & minimum values of current gain (hFE) can be obtained from the manufacturer's data sheet. Now $hFE(\text{max}) \ll hFE(\text{min})$ must be used to calculate the range of I_C & V_{CE} .

Q- Point shifts from active region to saturation when hFE is increased.

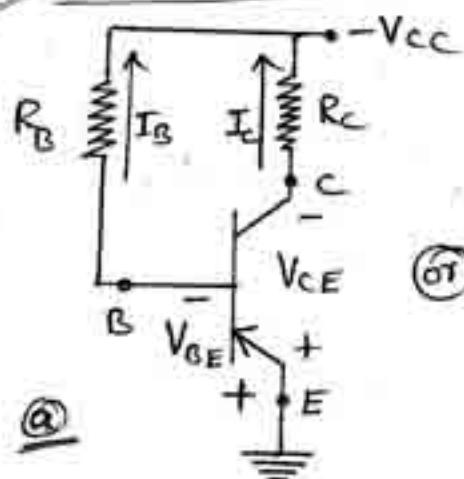
Eg. $I_C = 2mA$, $\beta = 100$ to 1000 , $V_{CE} = 10V$

→ V_{BE} & V_{CE} will change.

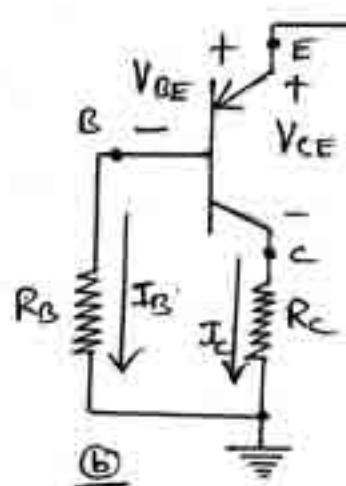
→ Voltage polarities & current directions are reversed compared to nPn transistor.

→ Eqs ⑥, ⑦ & ⑧ are used to analyze the circuit.

② Base bias using PNP transistor:



⑥



⑥

Fig ⑦: Base bias using a PNP transistor

③ Design of base-bias circuit:

Finding the component values of biasing circuit is called design.

Bias-circuit design can be done either in Mathematical approach or Characteristic approach.

Mathematical approach:

The values of V_{cc} , V_{CE} , V_{BE} , I_C (or I_a) & hFE will be given.

The design steps are as follows:

Step 1: calculate R_C using the relation

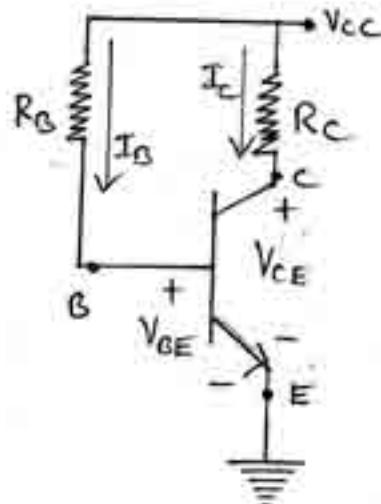
$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \quad - (1)$$

Step 2: calculate I_B (or I_C) using the relation,

$$I_C = \frac{I_C}{h_{FE}} \quad @ \quad I_C = h_{FE} I_B \quad - (2)$$

Step 3: calculate R_B using the relation.

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad - (3)$$



Fig(18): Base-bias circuit

④ DC load line & Q-point of Base-bias

Consider the base bias circuit as shown in fig(17)

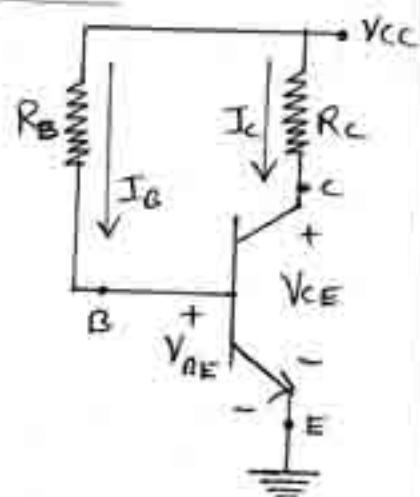
APPLYING KVL to collector-emitter loop.

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad - (22)$$

Put $I_C = 0$

$$V_{CE} = V_{CC} \quad - (23) \quad | \quad I_C = \frac{V_{CC}}{R_C} \quad - (24)$$

Point A($V_{CC}, 0$) Point B($0, \frac{V_{CC}}{R_C}$)



Fig(19): Base bias circuit

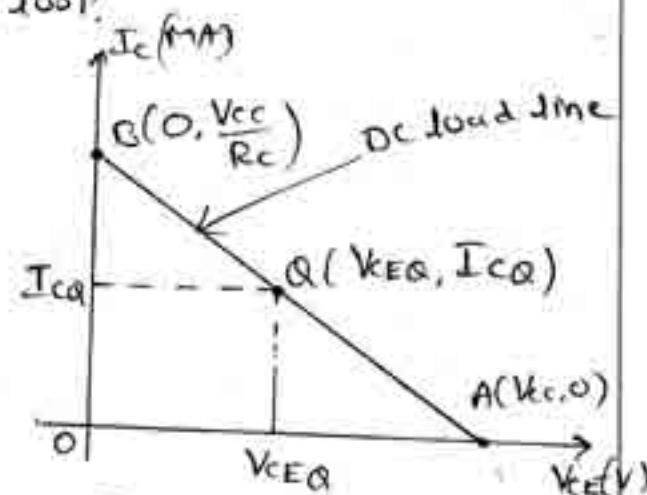
APPLYING KVL to base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad - (25)$$

$$\Rightarrow I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} \quad - (26)$$

$$\text{Let here, } I_C = I_{CQ} = \beta I_{BQ} \quad - (27)$$

$$\text{From (22), } V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_C \quad - (28)$$



Fig(20):

⑤ Advantages, disadvantages & Application of Base bias

Advantages @ Merits

- ① A very few number of components are required.
- ② operating point can be shifted easily anywhere in the active region by simply changing the base resistor (R_B).
- ③ There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages @ Demerits @ drawbacks

- ① Poor Stabilization (operating point is unstable)
- ② The stability factor is very high ($S = \beta + 1$), hence prone to thermal runaway.

APPLICATION @ USAGE

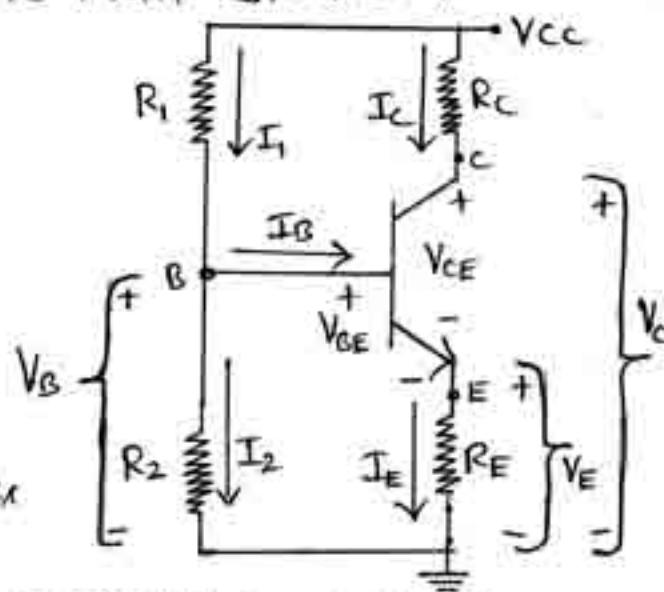
- ① Rarely used in linear circuits (ie the circuits which uses the transistor as a current source).
- ② It is often used in circuits where transistor is used as a switch.

⑥ Voltage - divider bias @ Self bias @ univocal bias @ Emitter current bias:

Voltage divider bias is the most stable transistor bias circuit.

Circuit operation

- A voltage divider bias circuit is shown in fig ②.
- Resistors R_1 & R_2 divide the supply voltage V_{CC} & voltage drop across R_2 provides biased bias voltage ' V_B ' at the base.



Fig(2): Voltage - divider bias circuit

- The emitter resistor R_E provides stabilization.
- The total dc load in series with the transistor is $(R_C + R_E)$
- Let the current I_2 is very much larger than I_B & V_B is assumed to be constant.

Methods of Analysis

- ① Approximate Method @ Analysis
- ② Exact @ Accurate @ Precise Method @ Analysis

① Approximate Method : (Fig 21)

It is a direct method, saves time & energy.

Applying KVL to Voltage-divisor network,

$$V_{CC} - I_1 R_1 - I_2 R_2 = 0 \quad - \textcircled{29}$$

$$\Rightarrow I_2 = \frac{V_{CC}}{R_1 + R_2} \quad - \textcircled{30} \quad \begin{aligned} &\text{Since } I_1 = I_B + I_2 \\ &\Rightarrow I_1 \approx I_2 \quad (\because I_2 \gg I_B) \end{aligned} \quad - \textcircled{31}$$

Voltage across R_2

$$V_B = I_2 R_2 \quad - \textcircled{32}$$

$$V_B = \frac{V_{CC}}{R_1 + R_2} R_2 \quad - \textcircled{33} \quad [\text{Using } \textcircled{30} \text{ in } \textcircled{32}]$$

$$\text{We have, } V_B = V_{BE} + V_E \quad - \textcircled{34}$$

$$\Rightarrow V_E = V_B - V_{BE} \quad - \textcircled{35}$$

$$\text{Emitter current, } I_E = \frac{V_E}{R_E} \quad - \textcircled{36} \quad [\text{Using } \textcircled{35} \text{ in } \textcircled{36}]$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \quad - \textcircled{37}$$

Applying KVL to Collector loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E) \quad - \textcircled{38} \quad [\because I_E \approx I_C]$$

Collector Voltage,

$$V_C = V_{CC} - I_C R_C \quad \text{or} \quad V_{CE} + V_E \quad - (39)$$

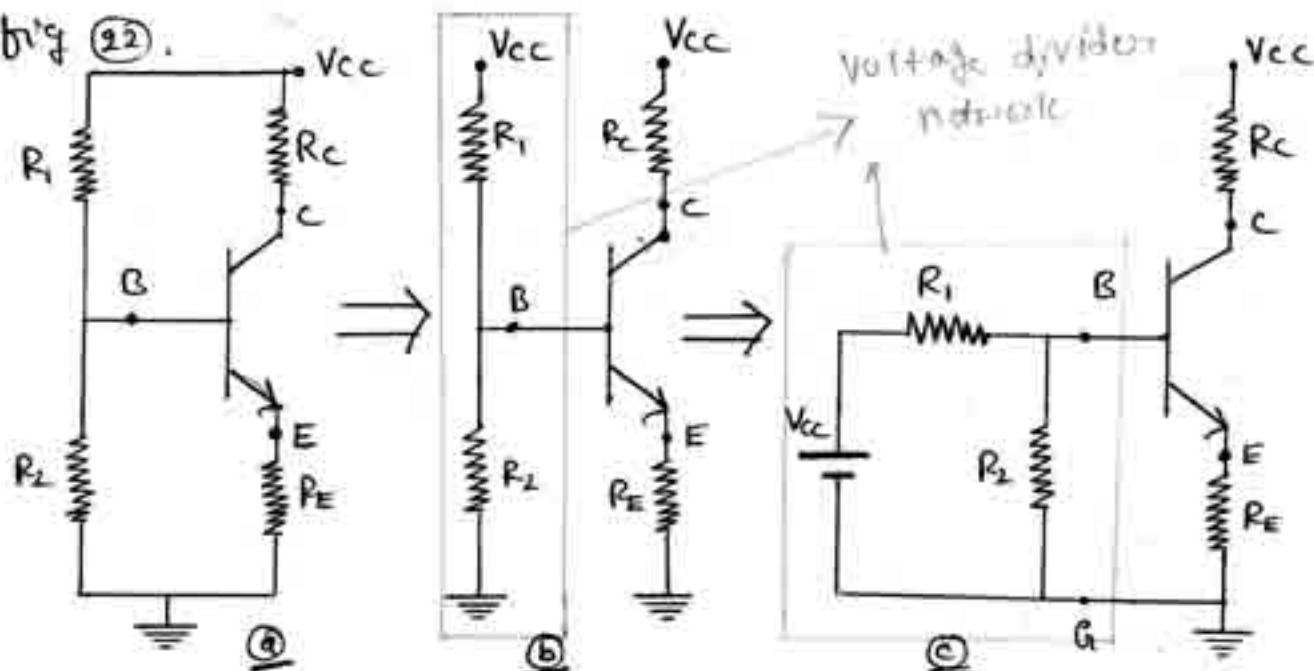
With I_C & I_E constant, the V_{CE} remains constant.
Q-point is independent of h_{FE} ($\because h_{FE}$ is not involved in any of the above equations)

② Exact ③ Accurate ④ Precise Method:

It can be applied to any voltage divider circuit.
The voltage-divider network is replaced by its
Thevenin equivalent circuit.

Consider the voltage divider bias circuit as shown in

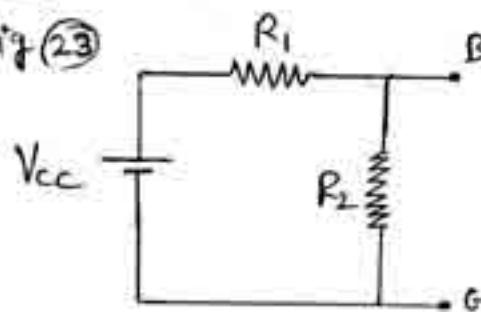
Fig (22).



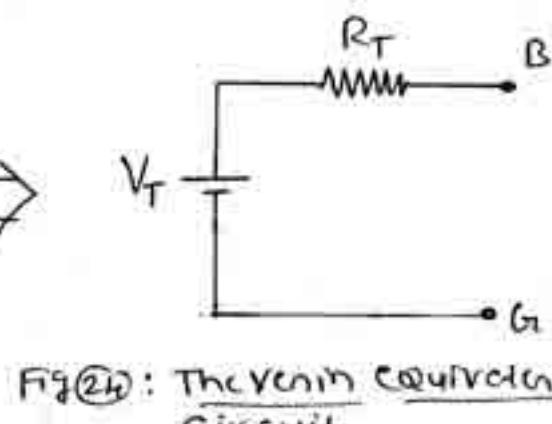
Fig(22): Simplification of voltage divider bias circuit

Now consider the voltage divider network as shown in

Fig(23)



Fig(23): Voltage divider network



Fig(24): Thevenin equivalent circuit

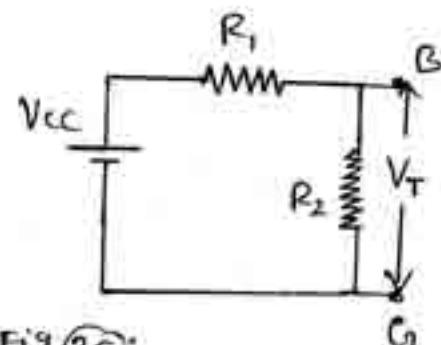
The Thevenin equivalent circuit of Voltage divider network is shown in fig 24.

V_T : Thevenin's voltage:

V_T is the voltage across B-E terminals @ Voltage across R_2 .

From Voltage divider rule.

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \quad -40$$

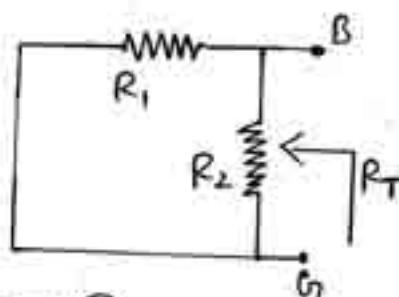


Fig(25):

R_T : Thevenin's resistance:

R_T is the resistance seen between the terminals B-G.
(By shorting the voltage source V_{CC})

$$\therefore R_T = \frac{R_1 R_2}{R_1 + R_2} \quad -41$$



Fig(26):

Now replace the voltage divider network with its Thevenin equivalent circuit (between B & G) as shown in fig 27

APPLYING KVL to base-emitter loop,

$$V_T - I_B R_T - V_{BE} - I_E R_E = 0$$

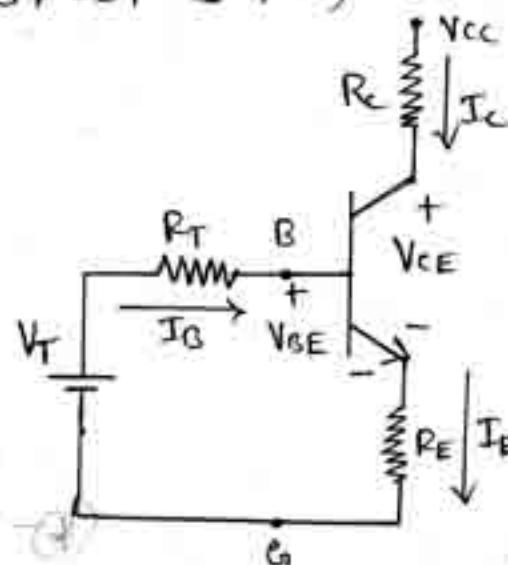
$$\Rightarrow V_T - V_{BE} = I_B R_T + I_E R_E$$

$$\Rightarrow V_T - V_{BE} = I_B R_T + (I_B + I_C) R_E$$

$$\Rightarrow V_T - V_{BE} = I_B R_T + (I_B + h_{FE} I_B) R_E$$

$$\Rightarrow V_T - V_{BE} = I_B [R_T + R_E (1 + h_{FE})]$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})} \quad -42$$



Fig(27): Voltage divider bias circuit with Thevenin equivalent circuit

$$\text{Now } I_c = h_{FE} I_B \quad -\textcircled{43}$$

APPLYING KVL to Collector - Emitter loop,

$$V_{CC} - I_c R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_c R_C - I_E R_E \quad -\textcircled{44}$$

Emitter Voltage,

$$V_E = I_E R_E \quad -\textcircled{45}$$

Collector Voltage,

$$V_C = V_{CE} + V_E \quad @ \quad V_C = V_{CC} - I_c R_C \quad -\textcircled{46}$$

$$\text{Base Voltage, } V_B = V_{BE} + V_E \quad -\textcircled{47}$$

(Q-Point is independent of h_{FE} (though h_{FE} is used in the above equations))

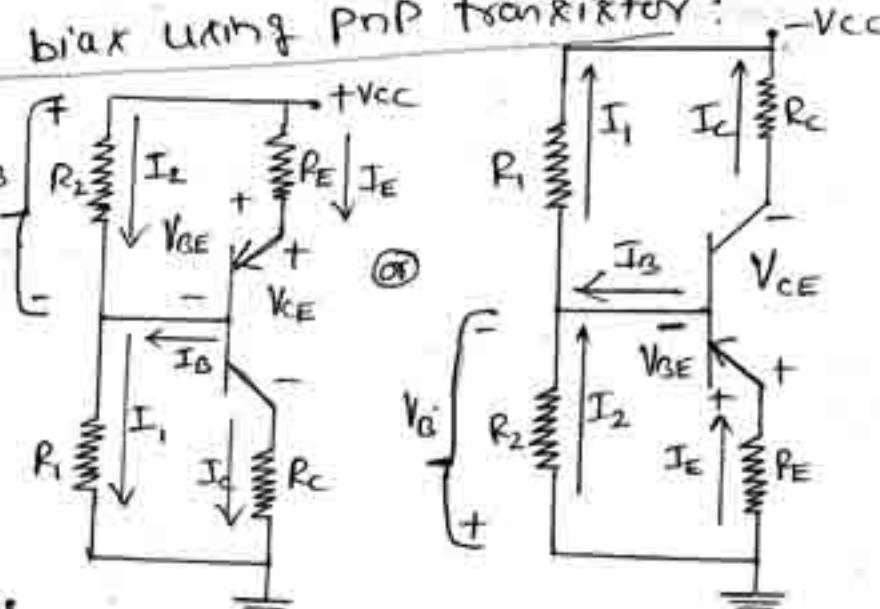
Note:

① Q-Point @ operating point is almost independent of h_{FE} (B) Variation. So voltage divider bias is the most stable transistor bias circuit. (See Numerical 15 & 16)

② Voltage divider bias using PNP transistor:

→ Voltage polarities V_C & current direction are reversed compared to n-p-n transistor.

→ A PNP transistor voltage divider bias circuit is analyzed in exactly the same way as an n-p-n transistor voltage divider bias circuit.



Fig(28): PNP transistor voltage divider bias circuit

③ The stability of a system (transistor circuit) is a measure of sensitivity of a network to variations in its parameters.

In any transistor amplifier, I_c is sensitive to the following parameters.

B: Increases with increase in temperature.

V_{BE} : Decreases about $7.5 \text{ mV}/^\circ\text{C}$ increase in temp.

I_{C0} (Reverse Saturation Current): Doubles for every 10°C increase in temperature.

(Q) Design of Voltage-divider bias circuit: (Finding R_1, R_2)
Reqd

The values of V_{cc} , V_{CE} , V_{BE} , I_c & h_{FE} will be given.

The design steps are as follows:

Step 1: Let $I_2 = \frac{I_c}{10}$ (As a thumb rule) - (48)

Step 2: Let $V_E \gg V_{BE}$ (If V_E is not given) - (49)

choose V_E in $3V$ - $5V$ range (3V when V_{cc} is $10\text{ to }9\text{V}$)
(5V regardless of voltage)

Step 3: Calculate R_E using the relation,

$$R_E = \frac{V_E}{I_c} \quad (\because I_c \approx I_E) \quad - (50)$$

Step 4: Calculate R_2 using the relation

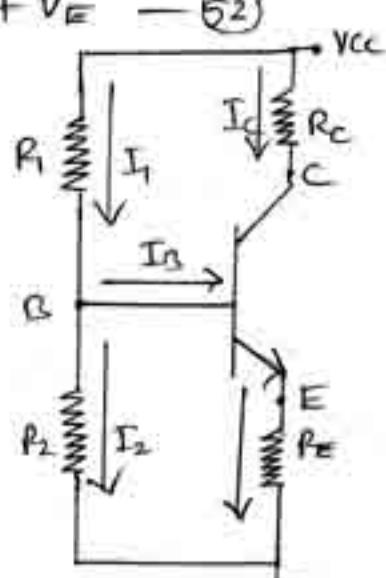
$$R_2 = \frac{V_B}{I_2} \quad \text{where, } V_B = V_{BE} + V_E \quad - (51)$$

Step 5: Calculate R_1 using the relation,

$$R_1 = \frac{V_{cc} - V_B}{I_2} \quad - (52)$$

Step 6: Calculate R_C using the relation,

$$R_C = \frac{V_{cc} - V_{CE} - V_E}{I_c} \quad - (54)$$



Fig(29): Voltage-divider bias circuit

⑤ DC load line & Q-point of Voltage-divider bias

→ Consider the Voltage-divider bias circuit as shown in fig ⑥

Applying KVL to collector-emitter loop.

$$V_{CC} - V_{CE} - I_c R_C - I_E R_E = 0$$

$$\Rightarrow V_{CC} - V_{CE} - I_c (R_C + R_E) = 0 \quad (\because I_c \approx I_E) \quad - \textcircled{55}$$

Put $I_c = 0$

$$V_{CE} = V_{CC} \quad - \textcircled{56}$$

Point A ($V_{CC}, 0$)

Put $V_{CE} = 0$

$$I_c = \frac{V_{CC}}{R_C + R_E} \quad - \textcircled{57}$$

$$\text{Point B } (0, \frac{V_{CC}}{R_C + R_E})$$

→ We have

$$I_E = \frac{V_B - V_{BE}}{R_E} \quad \text{where,}$$

$$V_B = \frac{V_{CC}}{R_1 + R_2}$$

~~$$\therefore I_c = I_{CQ} \approx I_E \quad - \textcircled{58}$$~~

~~$$\therefore V_{CE} = V_{CEQ} = V_{CC} - I_c (R_C + R_E) \quad - \textcircled{59}$$~~

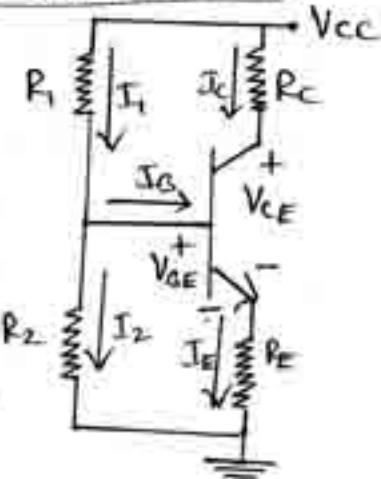


Fig ⑥: Voltage-divider bias circuit

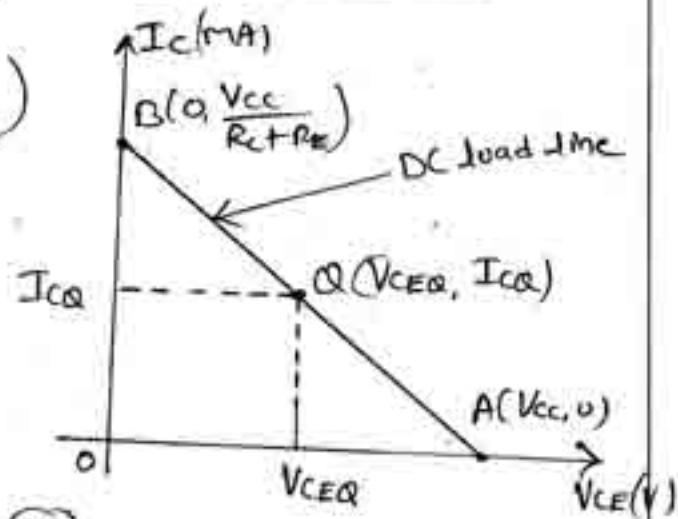


Fig ⑦

⑥ Which value of β to be used?

(a) Distinct B_{min} & B_{max} given

Solve using B_{min} & B_{max} separately

(b) Range of β given ($B_{min} - B_{max}$)

G.M @ geometric average of the two values & should be used.

$$\beta = \sqrt{B_{min} \times B_{max}}$$

⑦ Why Si is preferred over Ge?

Main reasons

(a) Smaller I_{CBO} : Si: 0.01 mA to 1 mA (At 25°C)
Ge: 2 to 15 mA

(b) Smaller variation of I_{CBO} with temperature:

- For Si: I_{CBO} approximately doublet with each $12^{\circ}\text{C}/\text{mV}$
 For Ge: I_{CBO} approximately doublet with each 8 to $10^{\circ}\text{C}/\text{mV}$.

④ Greater working temperature:

For Si: Normal working temperature upto 150°C

For Ge: Normal working temperature upto 70°C

⑤ Higher PIV rating:

Si: PIV rating around 1000V

Ge: PIV rating around 400V

[One drawback of Si as compared to Ge is Potential barrier of Si diode is 0.7V which is more than that of Ge diode (0.3V)]

⑥ Advantages, disadvantages & Applications of Voltage-divider bias:

Advantages @ Merits:

① Operating Point (α -Point) is almost independent of B (h_{FE}) variation.

② The Stability factor is the smallest possible value, ($S \approx 1$) hence leads to the maximum possible thermal stability. ③ Operating Point stabilized against shift in temperature.

Disadvantages @ Demerits @ drawbacks:

① It is complex, since it requires more components than other biasing circuit.

② If R_E is of large value, high V_{CC} is necessary. This increases cost as well.

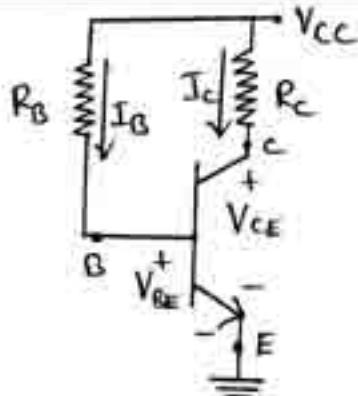
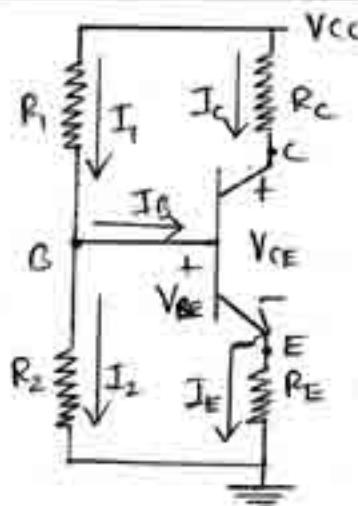
③ The negative feedback caused by R_E , reduces the

gain of the amplifier.

APPLICATIONS @ Usage

① Used to bias linear amplifier

② Composition of Biasing Circuits

Sl no.	Parameter	Bare bias	Voltage divider bias
1	Circuit		
2	Stability	Poor	Excellent
3	Bias Conditions	Unpredictable	More predictable
4	Feedback	Not present	Negative feedback
5	Components (Circuit Complexity)	Less	More
6	Stability Factor (S)	$S = 1 + \beta @ 1 + h_{FE}$	$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_E + R_M} \right)} \approx 1$ <p>Where $R_M = \frac{R_1 R_2}{R_1 + R_2}$</p>
7	$V_{CE(\min)}$	1.8V	9.4V
8	$V_{CE(\max)}$	13.75V	10.4V
9	I_C	$= \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$	$= \frac{V_{CC} R_2}{R_1 + R_2} - \frac{V_{BE}}{R_E}$

10	V_{CE}	$= V_{CC} - I_C R_C$	$= V_{CC} - I_C (R_C + R_E)$
11	DC Load line	A straight line from A($V_{CC}, 0$) to B($0, \frac{V_{CC}}{R_C}$)	Straight line from A($V_{CC}, 0$) to B($0, \frac{V_{CC}}{R_C + R_E}$)
12	Q-point	$Q(V_{CEO}, I_{CO})$ $V_{CEO} = V_{CC} - I_{CO} R_C$ $I_{CO} = \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \beta$	$Q(V_{CEO}, I_{CO})$ $V_{CEO} = V_{CC} - I_C (R_C + R_E)$ $I_{CO} = \frac{V_{CC} R_2}{R_1 + R_2} - \frac{V_{BE}}{R_E}$
13	Applications:-	Used in switching circuits	Used in linear amplification

Problems

1

- ① DRAW THE DC LOAD LINE FOR THE CIRCUIT SHOWN IN FIG 1@.

GIVEN CIRCUIT IS DRAWN BELOW.

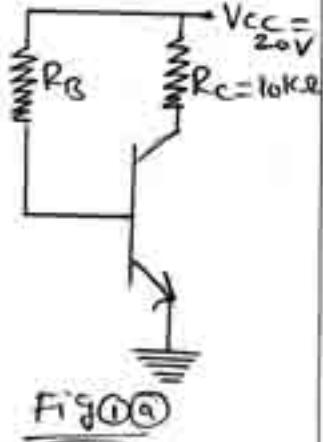
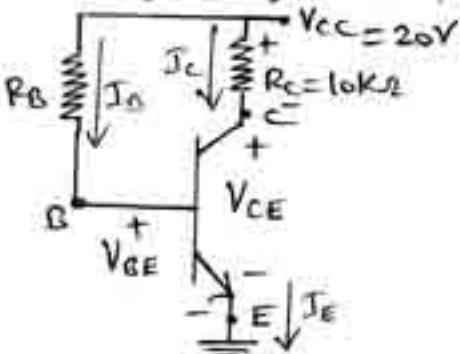


Fig 1@

APPLYING KVL TO COLLECTOR-EMITTER LOOP,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Put $I_C = 0$

$$V_{CE} = V_{CC} = 20V$$

Put $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{10 \times 10^3} = 2 \text{ mA}$$

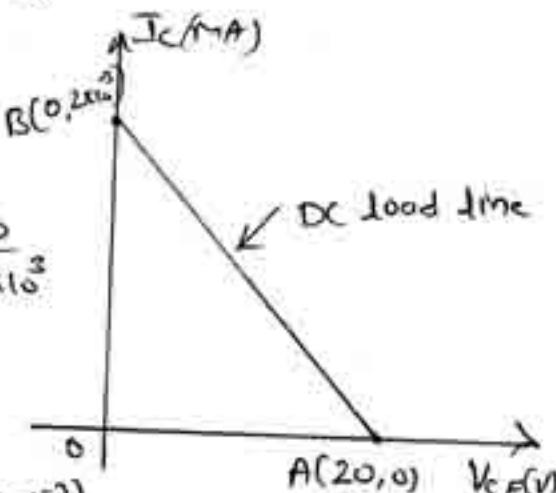
Mark at Point

$$A(V_{CE}, I_C) = A(20, 0)$$

Mark at Point

$$B(V_{CE}, I_C) = B(0, 2 \times 10^{-3})$$

DRAW A STRAIGHT LINE THROUGH $A(20, 0)$ & $B(0, 2 \times 10^{-3})$ TO GET LOAD LINE



- 2) THE TRANSISTOR CIRCUIT IN FIG 2@ HAS THE COLLECTOR CHARACTERISTICS SHOWN IN FIG 2@. DETERMINE THE CIRCUIT Q-POINT & ESTIMATE THE MAXIMUM SYMMETRICAL OUTPUT VOLTAGE SWING.

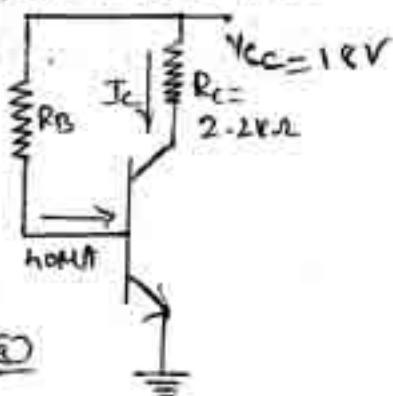


Fig 2@

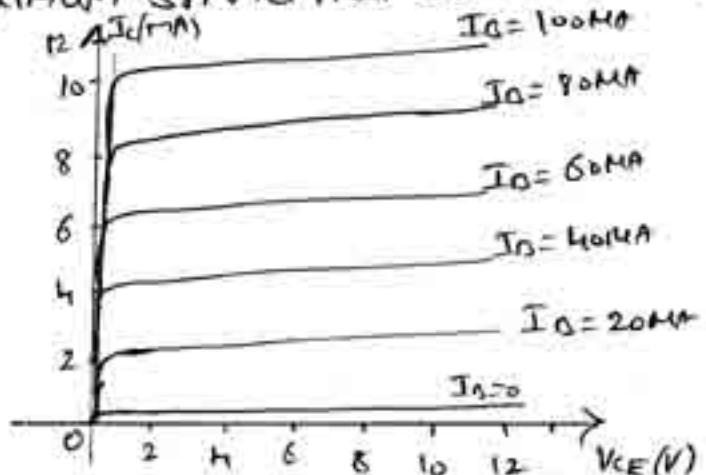


Fig 2@

- 3) APPLYING KVL TO COLLECTOR-EMITTER LOOP,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Put $I_C = 0$

$$V_{CE} = V_{CC} = 18V$$

Point A(18, 0)

Put $V_{CE} = 0$

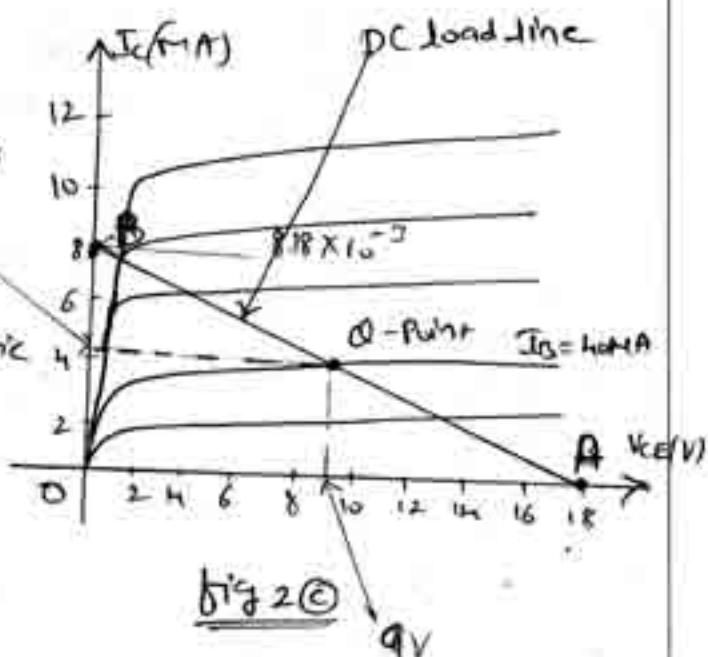
$$I_C = \frac{V_{CC}}{R_E} = \frac{18}{2.2 \times 10^3}$$

$$I_C = 8.18 \text{ mA}$$

$$\text{Point B}(0, 8.18 \times 10^{-3})$$

Draw the dc load line through points A & B on the given output characteristic [fig 2(b)].

The intersection of the dc load line & $I_C = 4.1 \text{ mA}$ characteristic is Q-Point as shown in fig 2(c).



The dc bias conditions are

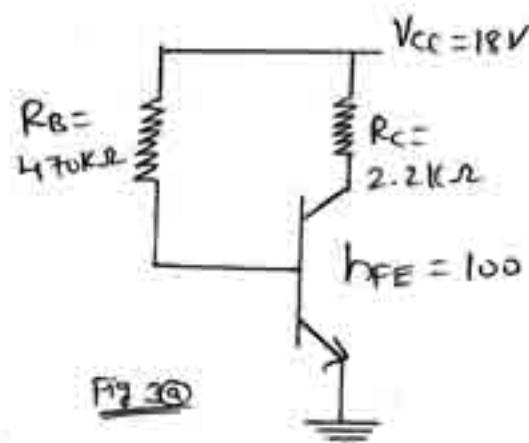
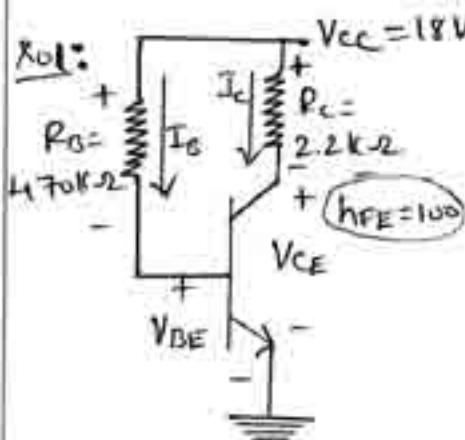
$$I_C \approx 4.1 \text{ mA} \quad \& \quad V_{CE} \approx 9V$$

∴ Maximum Symmetrical Output Voltage using it.

$$\boxed{\Delta V_{CE} \approx \pm 9V}$$

③

The base bias circuit is shown in fig 3(a). Determine I_B , I_C & V_{CE} .



APPLYING KVL to base-emitter circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18 - 0.7}{470 \times 10^3} = 36.8 \text{ mA}$$

$$\begin{aligned} V_{BE} &= 0.3V \text{ for Ge} \\ V_{BE} &= 0.7V \text{ for Si} \\ \text{If } V_{BE} \text{ not given take } V_{BE} &= 0.7V \end{aligned}$$

We have, $I_c = h_{FE} I_B = 100 \times 36.8 \times 10^{-6} = 3.68 \text{ mA}$

Applying KVL to collector-emitter loop,

$$V_{CE} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_c R_c = 18 - 3.68 \times 10^3 \times 2.2 \times 10^3$$

$$V_{CE} = 9.904 \text{ V}$$

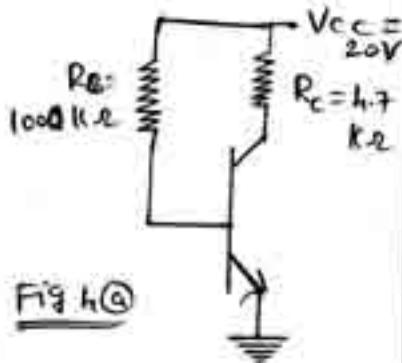
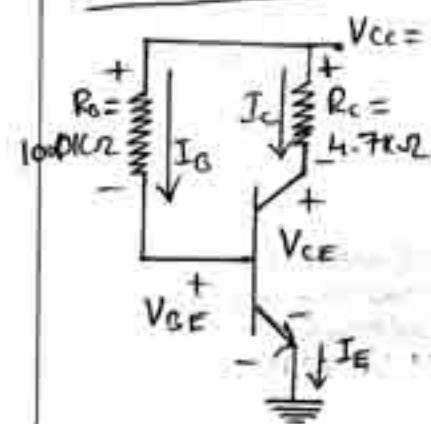


Fig 4(a)

- ④ For the circuit shown in fig 4(b), draw DC load line & mark the Q-point.
Assume $\beta = 100$ & neglect V_{BE}

Rot: DC load line



Step 1: Applying KVL to collector loop.

$$V_{CC} - I_c R_c - V_{CE} = 0$$

Step 2: Put $I_c = 0$, $V_{CE} = V_{CC} = 20V$

Mark as Point A($V_{CE}, 0$) = A(20, 0)

Step 3: Put $V_{CE} = 0$, $I_c = \frac{V_{CC}}{R_c} = \frac{20}{4.7 \times 10^3} = 4.25 \text{ mA}$

Mark as Point B($I_c, 0$) = B(4.25 × 10⁻³, 0)

Step 4: Draw a straight line through Points A & B, as shown in fig 4(b)

Q-Point

Step 1: Applying KVL to base-emitter loop,

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad (\text{Given } V_{BE} = 0)$$

$$\Rightarrow I_B = \frac{V_{CC}}{R_B} = \frac{20}{1 \times 10^6} = 20 \text{ nA}$$

We have

$$I_{eq} = \beta I_B = 100 \times 20 \times 10^{-9} = 2 \text{ mA}$$

Step 2: KVL to collector-emitter loop,

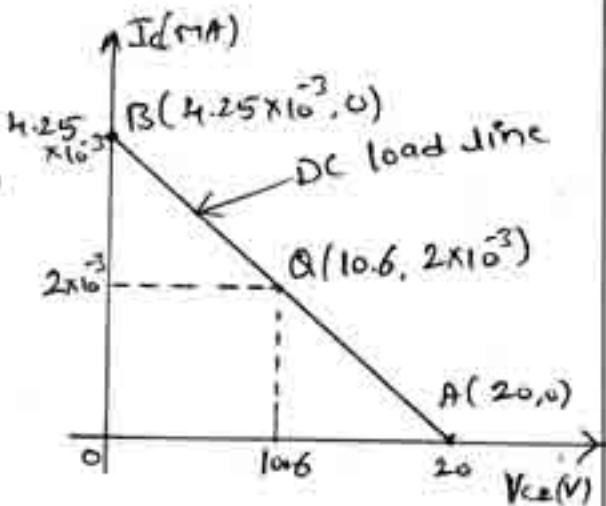


Fig 4(b)

$$V_{CE} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow V_{CEQ} = V_{CE} = V_{CC} - I_c R_c = 20 - 2 \times 10^{-3} \times 4.7 \times 10^3 = \underline{10.6V}$$

Mark at point Q ($10.6, 2 \times 10^{-3}$) [shown in fig 4(b)]

- ⑤ Calculate the value of R_B that will saturate the base bias transistor circuit. Given $h_{FE} = 200$, $V_{CE} = 0.3V$
 $R_C = 2.2k\Omega$, $V_{CC} = 10V$

sol: The base-bias circuit is shown in fig. 5

APPLYING KVL to collector-emitter loop.

$$V_{CC} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow I_c = \frac{V_{CC} - V_{CE}}{R_c} = \frac{10 - 0.3}{2.2 \times 10^3} = \underline{4.409mA}$$

Therefore,

$$I_C = h_{FE} I_B$$

$$\Rightarrow I_B = \frac{I_c}{h_{FE}} = \frac{4.409 \times 10^{-3}}{200}$$

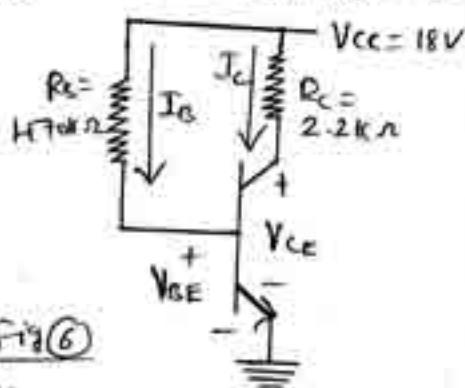
$$I_B = 22.04mA$$

APPLYING KVL to base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad (\text{ASSUME } V_{BE} = 0.7V)$$

$$\Rightarrow R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{22.04 \times 10^{-6}} = \underline{421.96k\Omega}$$

- ⑥ Calculate the maximum & minimum levels of I_C & V_{CE} for the base bias circuit shown in fig. 6 when $h_{FE(\text{min})} = 50$ & $h_{FE(\text{max})} = 200$.



sol: KVL to base loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18 - 0.7}{470 \times 10^{-3}} = \underline{36.8mA} \quad (\text{ASSUME } V_{BE} = 0.7V)$$

Fig(6)

For $h_{FE}(min)$

$$I_C = h_{FE(min)} I_A \\ = 50 \times 36.8 \times 10^{-6}$$

$$I_C = \underline{1.84 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - 1.84 \times 10^{-3} \times 2.2 \times 10^3 \\ = \underline{13.95 \text{ V}}$$

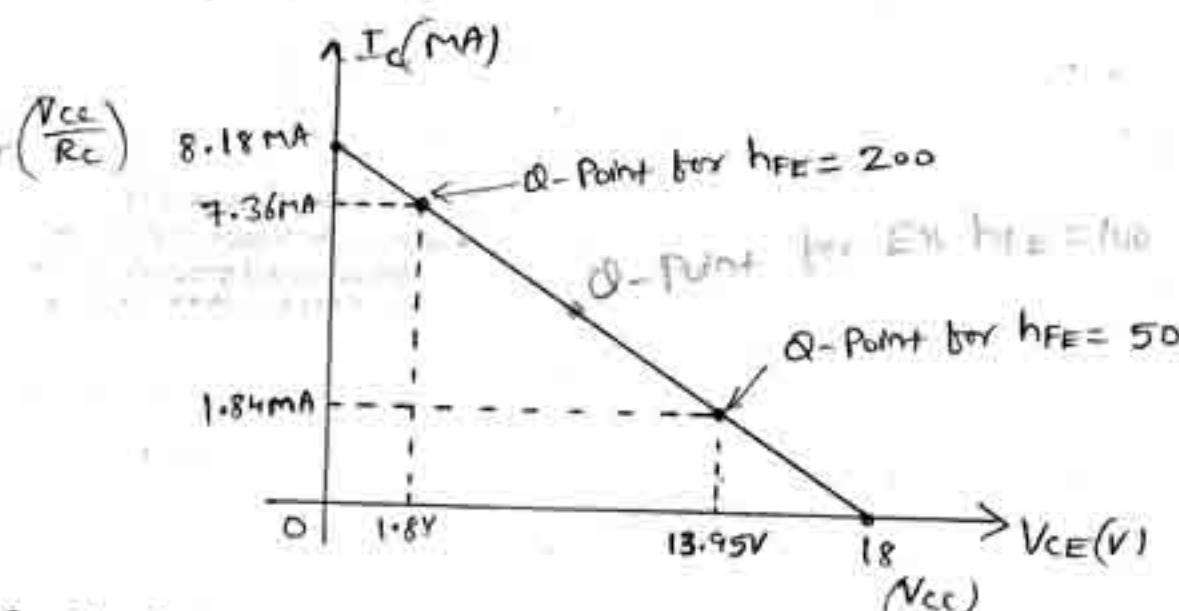
For $h_{FE}(max)$

$$I_C = h_{FE(max)} I_A \\ = 200 \times 36.8 \times 10^{-6}$$

$$= \underline{7.36 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - 7.36 \times 10^{-3} \times 2.2 \times 10^3 \\ = \underline{1.8 \text{ V}}$$



- Conclusion:
- From the above characteristics, the Q-point changes when $\beta(h_{FE})$ changes.
 - Q-Point shifts towards Saturation region (from active region) when h_{FE} is increased from 100 to 200
 - Q-Point shifts towards Cut-off region (from active region) when h_{FE} is decreased from 100 to 50.

- 3) Determine the following for the biased-biased configuration of bias. (a) Cut-off Voltage
 (b) I_{BQ} & I_{CQ} (c) Stability factor
 (d) V_{CEQ} (e) V_{CE} . (f) Saturation level

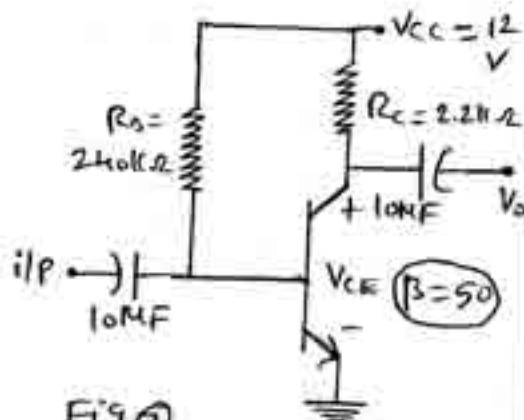


Fig ⑦

Q1 Neglect Capacitors.

(a) Applying KVL to base-emitter loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_B = I_{BQ} = \frac{V_{CE} - V_{BE}}{R_B}$$

$$\rightarrow I_{BQ} = \frac{12 - 0.7}{2.2 \times 10^3}$$

$$I_{BQ} = 47.08 \text{ mA}$$

We have,

$$I_{CQ} = \beta I_{BQ}$$

$$= 50 \times 47.08 \times 10^{-6}$$

$$I_{CQ} = 2.35 \text{ mA}$$

$$\textcircled{1} \quad V_{BC} = V_B - V_C = 0.7 - 6.83 = -6.13 \text{ V}$$

(c) Saturation level (d) Saturation Current.

(e) Stability factor

$$S = 1 + \beta = 51$$

$$\textcircled{2} \quad V_{CE}(\text{cut-off}) = V_{CC} = 12 \text{ V}$$

Fig 8 shows biasing with base resistor method.

i) Determine I_C & V_{CE} . Neglect small base-emitter voltage. Given $\beta = 50$

ii) If R_B is changed to $50\text{k}\Omega$, find the new operating point

iii)

Applying KVL to base loop,

$$V_{BE} - I_B R_B - V_{BE} = 0 \quad \text{--- (1)}$$

$$\Rightarrow I_B = \frac{V_{BE}}{R_B} = \frac{2}{100 \times 10^3} = 20 \text{ mA} \quad (\text{Given } V_{BE} = 0)$$

$$\text{Now } I_C = \beta I_B = 50 \times 20 \times 10^{-6} = 1 \text{ mA}$$

Applying KVL to collector loop.

(f) KVL to collector-emitter loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$V_{CEQ} = V_{CE} = 12 - 2.35 \times 10^3 \times 2.2 \times 10^3$$

$$V_{CEQ} = 6.83 \text{ V}$$

$$\textcircled{3} \quad V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{CE} = 6.83 \text{ V}$$

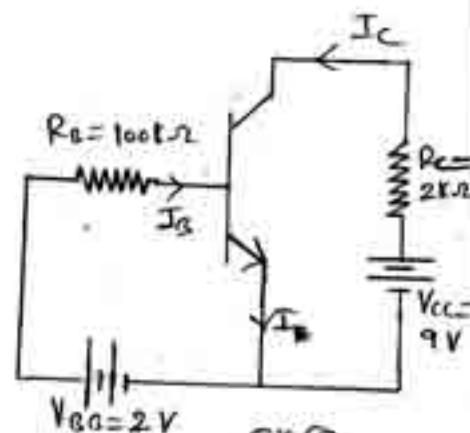


Fig 8

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad \text{--- (2)}$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C = 9 - 1 \times 10^{-3} \times 2 \times 10^3 = \underline{\underline{7V}}$$

(ii) From (1),

$$I_B = \frac{V_{BE}}{R_B} = \frac{2}{50 \times 10^3} = 40 \mu\text{A}$$

Now, $I_C = \beta I_B = 50 \times 40 \times 10^{-6} = 2 \text{mA} //.$

$$V_{CE} = V_{CC} - I_C R_C = 9 - 2 \times 10^{-3} \times 2 \times 10^3 = 5 \text{V} //.$$

New operating point is (5V, 2mA)

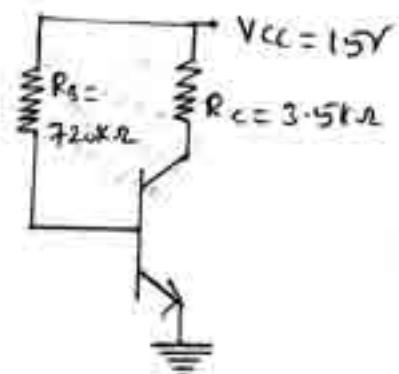
- Q) Design base resistor bias circuit for $V_{CE} = 8 \text{V}$, $I_C = 2 \text{mA}$. Given $V_{CC} = 15 \text{V}$, $\beta = 100$ (Si transistor), $V_{BE} = 0.6 \text{V}$. Also calculate the load resistance.

- Given $V_{CE} = 8 \text{V}$, $I_C = 2 \text{mA}$, $V_{CC} = 15 \text{V}$, $\beta = 100$, $V_{BE} = 0.6 \text{V}$

We have $R_C = \frac{V_C - V_{CE}}{I_C} = \frac{15 - 8}{2 \times 10^{-3}} = \underline{\underline{3.5 \text{k}\Omega}} \quad (\text{Load resistance})$

$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15 - 0.6}{0.02 \times 10^{-3}} = \underline{\underline{720 \text{k}\Omega}}$ $\left(I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{100} = 0.02 \text{mA} \right)$

Fig (9) Rhombus base transistor bias Ckt.



- Q) A base bias circuit in fig (10) is subjected to an increase in temperature from 25°C to 75°C . If $\beta = 100$ at 25°C & 150 at 75°C , determine the percentage change in Q-point values over this temperature range. Neglect change in V_{BE} & the effect of leakage current.

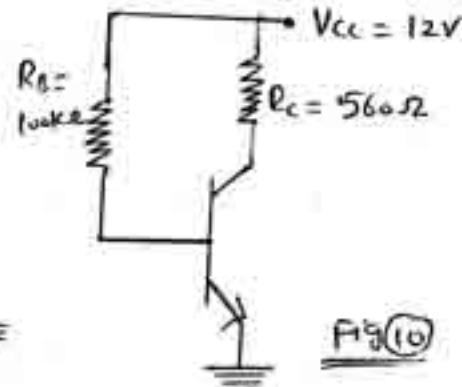


Fig (10)

Ques: At 25°C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{100 \times 10^3} = 0.113 \text{ mA}$$

$$I_C = \beta I_B = 100 \times 0.113 \times 10^{-3} = 11.3 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 12 - 11.3 \times 10^{-3} \times 560$$

$$V_{CE} = \underline{5.67 \text{ V}}$$

At 75°C

$$I_B = \frac{12 - 0.7}{100 \times 10^3} = 0.113 \text{ mA}$$

$$I_C = \beta I_B = 150 \times 0.113 \times 10^{-3}$$

$$I_C = 17 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - 17 \times 10^{-3} \times 560$$

$$= \underline{2.48 \text{ V}}$$

Yage Change in I_C is,

$$\Delta I_C (\%) = \frac{I_C (75^{\circ}\text{C}) - I_C (25^{\circ}\text{C})}{I_C (25^{\circ}\text{C})} \times 100$$

$$= \frac{17 \times 10^{-3} - 11.3 \times 10^{-3}}{11.3 \times 10^{-3}} \times 100$$

$$= \underline{50\% \text{ (Increase)}} \quad \left(\begin{array}{l} I_C \text{ changes by the} \\ \text{same percentage as } \beta \end{array} \right)$$

Yage change in V_{CE} is,

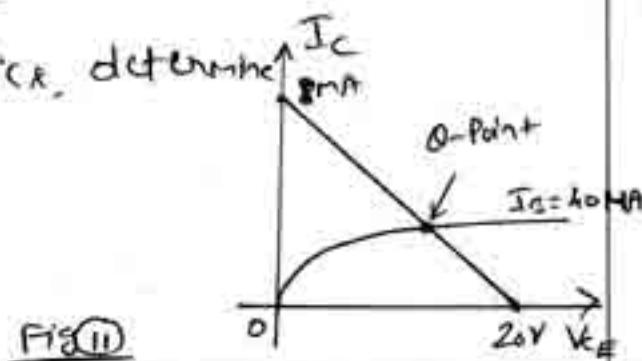
$$\Delta V_{CE} (\%) = \frac{V_{CE} (75^{\circ}\text{C}) - V_{CE} (25^{\circ}\text{C})}{V_{CE} (25^{\circ}\text{C})} \times 100$$

$$= \frac{2.48 - 5.67}{5.67} \times 100$$

$$= \underline{-56.3\% \text{ (Decrease)}}$$

Comments: Q-Point is extremely dependent on β . Therefore, base bias circuit is very unstable.

- II) Fig (II) shows the characteristic. determine V_{CC} , R_C & R_B . (Base bias circuit)



Q1: From the dc load line (given), $V_{CC} = 20V$

$$I_C = \frac{V_{CC}}{R_C} @ R_C = \frac{V_{CC}}{I_C}$$

$$R_C = \frac{20}{8 \times 10^3}$$

We have, $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$$R_C = 2.5k\Omega$$

($V_{CC} R_C = 2.4k\Omega$ Standard Value)

$$\Rightarrow R_B = \frac{20 - 0.7}{400 \times 10^{-6}} \quad (\text{From the characteristic,})$$

$$I_B = 40mA$$

$$R_B = \underline{482.5k\Omega} \quad (V_{CC} R_C = 470k\Omega \text{ Standard Value})$$

- Q2: A base bias circuit has $V_{CC} = 20V$, $R_B = 400k\Omega$, $R_C = 2.2k\Omega$, $V_{CE} = 2V$. Calculate β . Determine the new V_{CE} when a new transistor with $\beta = 100$ is used.

Sol: Given $V_{CC} = 20V$, $R_B = 400k\Omega$, $R_C = 2.2k\Omega$, $V_{CE} = 2V$, $\beta = ?$

We have,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{20 - 2}{2.2 \times 10^3} = 8.181mA$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{400 \times 10^3} = 48.25mA$$

Now, $\beta (h_{FE}) = \frac{I_C}{I_B} = \frac{8.181 \times 10^{-3}}{48.25 \times 10^{-6}} = 169.55 //$

Now $V_{CE} = ?$, $\beta = 100$

$$I_C = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{400 \times 10^3} = 48.25mA$$

$$I_C = h_{FE} I_B = 100 \times 48.25 \times 10^{-6} = 4.825mA$$

$$V_{CE} = V_{CC} - I_C R_C = 20 - 4.825 \times 10^{-3} \times 2.2 \times 10^3$$

$$V_{CE} = \underline{9.385V}$$

- ③ Analyze the voltage-divider bias circuit shown in fig ⑬ to determine the emitter voltage, collector voltage, & collector-emitter voltage.

- ④ Accurately analyze fig ⑬ to determine I_C , V_E , V_C & V_{CE} when $h_{FE} = 100$

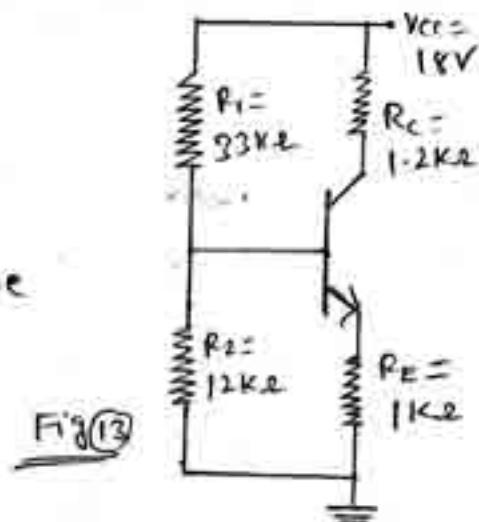


Fig ⑬

Q3 We have $V_B = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 4.8V$

$V_E = V_B - V_{BE} = 4.8 - 0.7 = 4.1V$

$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4.8 - 0.7}{1 \times 10^3} = 4.1mA //, I_C \approx I_E = 4.1mA$

$V_C = V_{cc} - I_C R_c = 18 - 4.1 \times 10^{-3} \times 1.2 \times 10^3 = 13.1V$

$V_{CE} = V_C - V_E = 13.1 - 4.1 = 9V$

Q4 We have $V_T = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 4.8V$

$R_T = R_1 || R_2 = 33 \times 10^3 || 12 \times 10^3 = 8.8k\Omega$

$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})} = \frac{4.8 - 0.7}{8.8 \times 10^3 + 1 \times 10^3 (1 + 100)} = 37.3mA //$

$I_C = h_{FE} I_B = 100 \times 37.3 \times 10^{-6} = 3.73mA //$

$I_E = I_B + I_C = 37.3 \times 10^{-6} + 3.73 \times 10^{-3} = 3.77mA //$

$V_E = I_E R_E = 3.77 \times 10^{-3} \times 1 \times 10^3 = 3.77V //$

$V_C = V_{cc} - I_C R_c = 18 - 3.73 \times 10^{-3} \times 1.2 \times 10^3 = 13.52V$

$V_{CE} = V_C - V_E = 13.52 - 3.77 = 9.75V$

O-point if $\Omega(V_{CE}, I_C) = \Omega(9.75, 3.73 \times 10^{-3})$

- ④ (a) Accurately analyze the Voltage-divider bias circuit shown in fig ④
for $h_{FE}(\min) = 50$

- (b) Repeat Part (a) for $h_{FE}(\max) = 200$

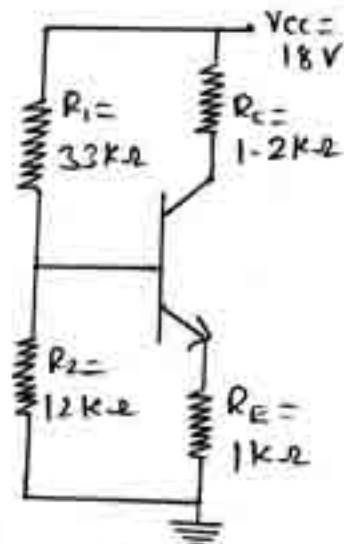


Fig ④

Given
④ (a) We have $V_T = \frac{V_{CC}}{R_1 + R_2} = \frac{18}{33 \times 10^3 + 12 \times 10^3} = 4.8V$

$$R_T = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{33 \times 10^3 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 8.8k\Omega$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})} = \frac{4.8 - 0.7}{8.8 \times 10^3 + 1 \times 10^3(1 + 50)} = 68.6mA$$

$$I_C = h_{FE} I_B = 50 \times 68.6 \times 10^{-3} = 3.43mA$$

$$I_E = I_B + I_C = 68.6 \times 10^{-3} + 3.43 \times 10^{-3} = 3.5mA$$

$$V_E = I_E R_E = 3.5 \times 10^{-3} \times 1 \times 10^3 = 3.5V$$

$$V_C = V_{CC} - I_C R_C = 18 - 3.43 \times 10^{-3} \times 1.2 \times 10^3 = 13.9V$$

$$V_{CE} = V_C - V_E = 13.9 - 3.5 = 10.4V$$

$$\text{Q-Point } Q(V_{CE}, I_C) = Q(10.4, 3.43 \times 10^{-3})$$

- ⑤ We have

$$V_T = 4.8V, R_T = 8.8k\Omega$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1 + h_{FE})} = \frac{4.8 - 0.7}{8.8 \times 10^3 + 1 \times 10^3(1 + 200)} = 19.5mA$$

$$I_C = h_{FE} I_B = 200 \times 19.5 \times 10^{-3} = 3.9mA$$

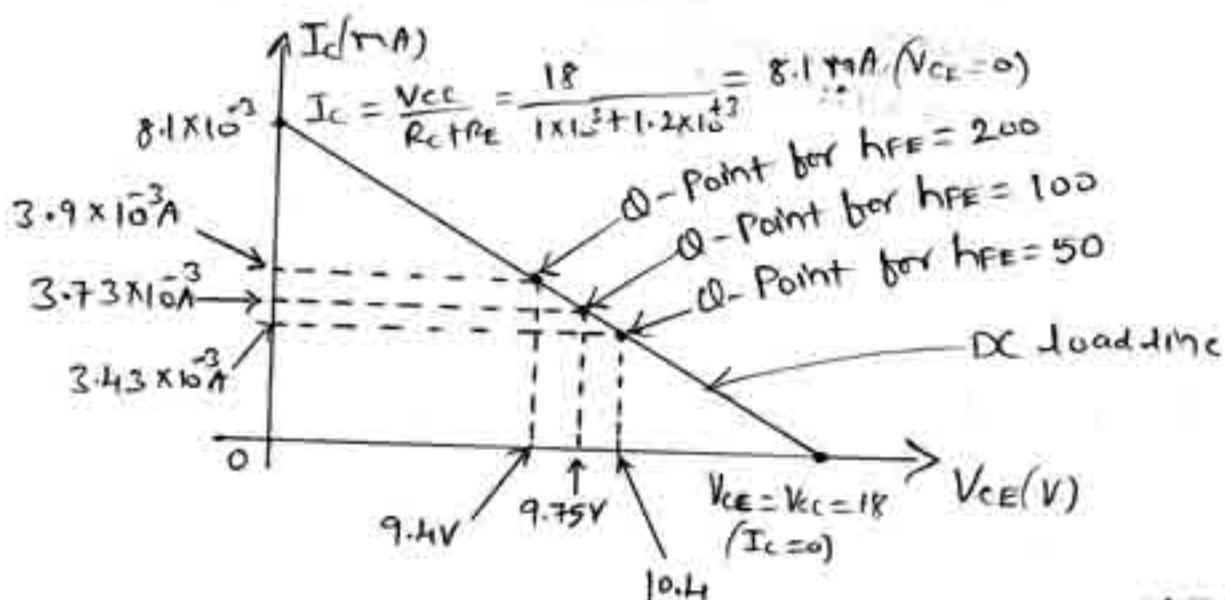
$$I_E = I_C + I_E = 19.5 \times 10^{-6} + 3.9 \times 10^{-3} = 3.92 \text{ mA}$$

$$V_E = I_E R_E = 3.92 \times 10^{-3} \times 1 \times 10^3 = 3.92 \text{ V}$$

$$V_C = V_{CC} - I_C R_C = 18 - 3.9 \times 10^{-3} \times 1.2 \times 10^3 = 12.3 \text{ V}$$

$$V_{CE} = V_C - V_E = 12.3 - 3.92 = 9.4 \text{ V}$$

O-Point, Q(V_{CE}, I_C) = Q(9.4, 3.9 × 10⁻³)



Conclusion: • From the above characteristic, the circuit (Voltage divider bias) is insensitive to the change in β .

(ii) O-Point is most insensitive to changes in β .

∴ Voltage-divider bias circuit is most stable bias circuit.

- 15) For the Fig 15, draw the dc load line & determine the operating point. Assume Si transistor.

RQ1: DC load line

Redraw the given circuit

Applying KVL to collector -

Emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CC} - V_{CE} - I_C (R_C + R_E) = 0 \quad \text{--- (1)}$$

(Since $I_E \approx I_C$)

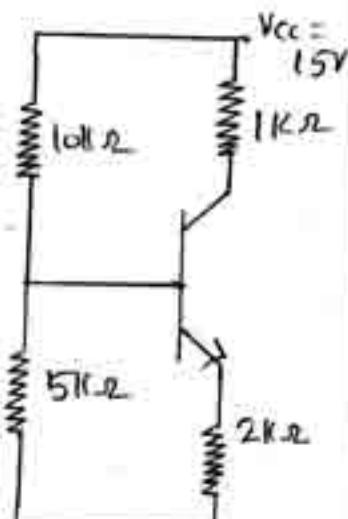
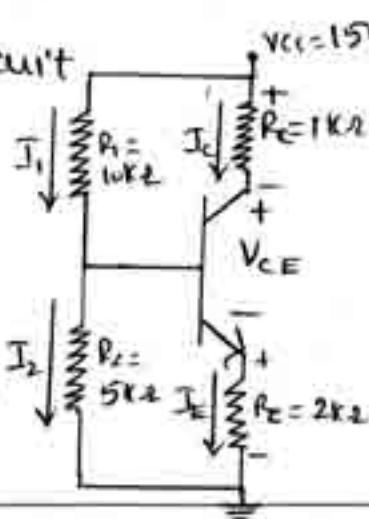


Fig 15

① Put $I_c = 0$ in ①

$$V_{CE} = V_{CC} = 15V$$

Mark at Point A (V_{CE}, I_c) = A(15, 0)

② Put $V_{CE} = 0$ in ①

$$I_c = \frac{V_{CC}}{R_C + R_E} = \frac{15}{1 \times 10^3 + 2 \times 10^3} = 5mA$$

Mark at Point B (V_{CE}, I_c) = B(0, 5mA)

DRAW a straight through A(15, 0) & B(0, 5mA) to get DC load line as shown in fig 15@

Operating Point (Q-Point)

VT across R_2 ,

$$\begin{aligned} V_B &= \frac{V_{CC}}{R_1 + R_2} \\ &= \frac{15 \times 5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \end{aligned}$$

$$\underline{V_B = 5V}$$

Emitter current,

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \times 10^3} = 2.15mA$$

Collector current.

$$(I_{CQ} =) I_c \approx I_E = 2.15mA //$$

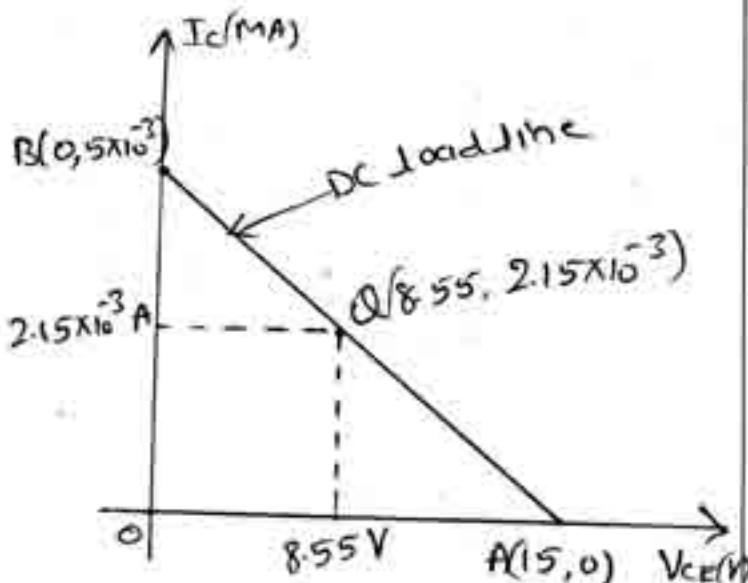
Collector-emitter Voltage,

$$\begin{aligned} (V_{CEQ} =) V_{CE} &= V_{CC} - I_c(R_C + R_E) \\ &= 15 - 2.15 \times 10^3 (1 \times 10^3 + 2 \times 10^3) \\ &= 8.55V \end{aligned}$$

\therefore Q-Point is $Q(V_{CEQ}, I_{CQ}) = Q(8.55, 2.15 \times 10^{-3})$

Mark operating point at $Q(8.55, 2.15 \times 10^{-3})$

- Q) A Potential divider bias circuit has $R_1 = 50k\Omega$, $R_2 = 10k\Omega$, $R_E = 1k\Omega$. If $V_{CC} = 12V$, find
 ④ Stability factor. ($B = 100$)
 ⑤ the value of I_c , given $V_{BE} = 0.7V$. ⑥ Saturation current ($R_C = 1.2k\Omega$)
 ⑦ I_c , given $V_{BE} = 0.3V$ ⑧ comment on the results.



(a) Given $R_1 = 50 \times 10^3 \Omega$, $R_2 = 10 \times 10^3 \Omega$, $R_E = 1 \times 10^3 \Omega$; $V_{CC} = 12V$

$$\textcircled{a} \quad V_B = \frac{V_{CC}}{R_1 + R_2} = \frac{12}{50 \times 10^3 + 10 \times 10^3} = 2V$$

$$\text{Collector current, } I_C = \frac{V_B - V_{BE}}{R_E} = \frac{2 - 0.1}{1 \times 10^3} = 1.9 \text{ mA} //$$

$$\textcircled{b} \quad V_B = 2V$$

$$I_C = \frac{V_B - V_{BE}}{R_E} = \frac{2 - 0.3}{1 \times 10^3} = 1.7 \text{ mA} //$$

\textcircled{c} V_{BE} varies by 200%. The value of I_C changes by nearly 10%.. \therefore In Voltage-divider bias circuit, I_C is almost independent of transistor parameter variations.

$$\textcircled{d} \quad S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_E + R_{TH}} \right)} = \frac{1 + 100}{1 + 100 \left(\frac{1 \times 10^3}{1 \times 10^3 + 8.33 \times 10^3} \right)}$$

$$S = 8.6 //$$

$$\begin{aligned} R_{TH} &= \frac{R_1 R_2}{R_1 + R_2} \\ &= \frac{50 \times 10^3}{(50 + 10) \times 10^3} \\ &= 8.33 \text{ k}\Omega \end{aligned}$$

$$\textcircled{e} \quad I_{CSat} = \frac{V_{CC}}{R_{TH} + R_E} = \frac{12}{1.2 \times 10^3 + 1 \times 10^3} = 5.45 \text{ mA}$$

\textcircled{f} (a) Determine the dc bias voltage V_{CE} & the current I_C for the voltage-divider circuit of fig (f)

(b) Repeat the analysis of fig (f) using the approximate technique & compare solutions for I_C & V_{CE} .

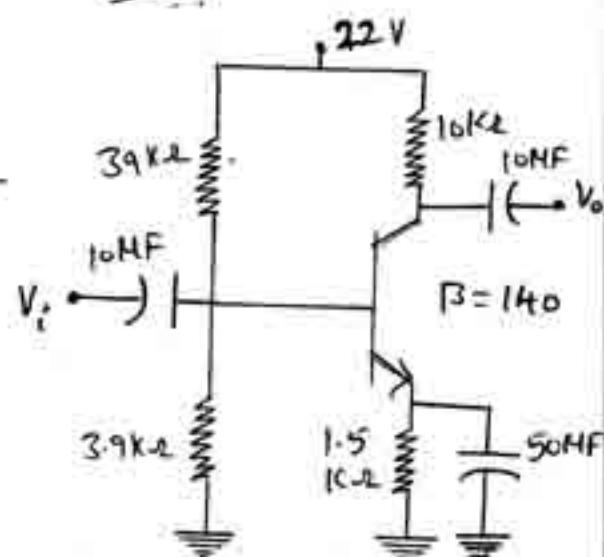


Fig (f)

(a) $V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22(3.9 \times 10^3)}{39 \times 10^3 + 3.9 \times 10^3} = \underline{\underline{2V}}$

$$R_T = \frac{R_1 R_2}{R_1 + R_2} = \frac{39 \times 10^3 \times 3.9 \times 10^3}{39 \times 10^3 + 3.9 \times 10^3} = \underline{\underline{3.55k\Omega}}$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1+h_{FE})} = \frac{2 - 0.7}{3.55 \times 10^3 + 1.5 \times 10^3 (141)} = \underline{\underline{6.05mA}}$$

$$I_C = h_{FE} I_B = 140 \times 6.05 \times 10^{-6} = 0.85 \text{ mA}. \quad (I_E = I_B + I_C \\ = 0.85 \text{ mA} = I_C)$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 22 - 0.85 \times 10^{-3} / 10 \times 10^3 + 1.5 \times 10^3$$

$$V_{CE} = 12.22V$$

(b) $V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22 \times 3.9 \times 10^3}{39 \times 10^3 + 3.9 \times 10^3} = \underline{\underline{2V}}$

$$V_E = V_B - V_{BE} = 2 - 0.7 = \underline{\underline{1.3V}}$$

$$(I_{CQ} =) \quad I_C \approx I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.3}{1.5 \times 10^3} = 0.867 \text{ mA}$$

$$(V_{CEQ} =) \quad V_{CE} = V_{CC} - I_C (R_C + R_E) = 22 - 0.867 \times 10^{-3} (10k + 1.5k)$$

$$(V_{CEQ}) V_{CE} = 12.03V$$

Comparison:

Analytical	$I_{CQ}(I_C)$	$V_{CEQ}(V_{CE})$
Exact	0.85mA	12.22V
Approximate	0.867mA	12.03V

The values of I_{CQ} & V_{CEQ} are very close. (The larger the value of R_1 compared to R_2 , the closer the approximate to the exact solution).

- 8) Design a base bias circuit to have $V_{CE} = 5V$, $I_C = 5mA$. The supply voltage is 15V, $h_{FE} = 100$

$$\text{Ans: } R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{15 - 5}{5 \times 10^{-3}} = 2k\Omega //$$

(V_{RE} 1.8k Ω @ 2.2k Ω Standard Value)

$$I_B = \frac{I_E}{h_{FE}} = \frac{5 \times 10^{-3}}{100} = 50\text{mA}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15 - 0.7}{50 \times 10^{-6}} = 286k\Omega //$$

(V_{RE} 270k Ω @ 330k Ω Standard Value)

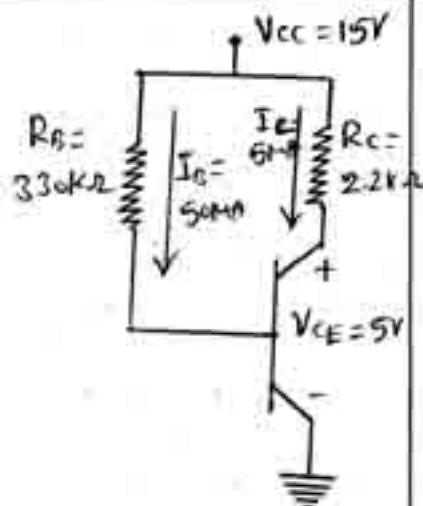


Fig 18

The biasing circuit is shown in Fig 18

- Q) Given $I_{CO} = 2\text{mA}$ & $V_{CEO} = 10\text{V}$. determine R_1 & R_C of Potential divider circuit shown in Fig 19

Sol: $V_E = I_E R_E = 2 \times 10^{-3} \times 1.2 \times 10^3 = 2.4\text{V}$
 $(\because I_C \approx I_E)$

$$V_o = V_{BE} + V_E = 0.7 + 2.4 = 3.1\text{V}$$

$$V_o = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$\Rightarrow 3.1 = \frac{18 \times 18 \times 10^3}{R_1 + 18 \times 10^3}$$

$$\Rightarrow R_1 = 86.52\text{k}\Omega \quad (V_{RE} 82\text{k}\Omega @ 91\text{k}\Omega \text{ Standard Value})$$

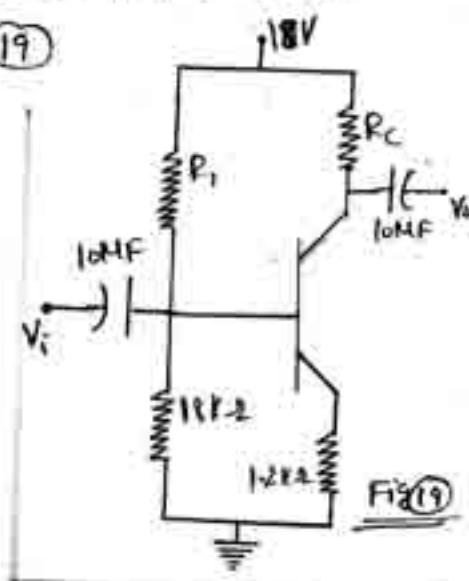


Fig 19

$$V_C = V_{CE} + V_E = 10 + 2.4 = 12.4\text{V}$$

$$R_C = \frac{V_{CC} - V_{CE} - R_E}{I_C} \quad @ \quad \frac{V_{CC} - V_C}{I_C}$$

$$= \frac{18 - 10}{2 \times 10^{-3}} - 1.2 \times 10^3$$

$$R_C = 2.8\text{k}\Omega //$$

- Q) Design the voltage divider bias circuit to have $V_{RE} = V_E = 5\text{V}$ & $I_C = 5\text{mA}$ when the supply voltage is 15V. Assume $h_{FE} = 100$.

Given $V_{CE} = 5V$, $V_E = 5V$, $I_C = 5mA$, $hFE = 100$. $V_{CC} = 15V$
 Assume $V_{BE} = 0.7V$.

Step 1: Let $I_2 = I_c = \frac{5 \times 10^{-3}}{10} = \underline{\underline{500\text{nA}}}$

Step 2: $R_E = \frac{V_E}{I_c} = \frac{5}{5 \times 10^{-3}} = \underline{\underline{1\text{k}\Omega}}$

Step 3: $R_2 = \frac{V_B}{I_2} = \frac{V_{BE} + V_E}{I_2} = \frac{0.7 + 5}{500 \times 10^{-6}} = \underline{\underline{11.4\text{k}\Omega}}$

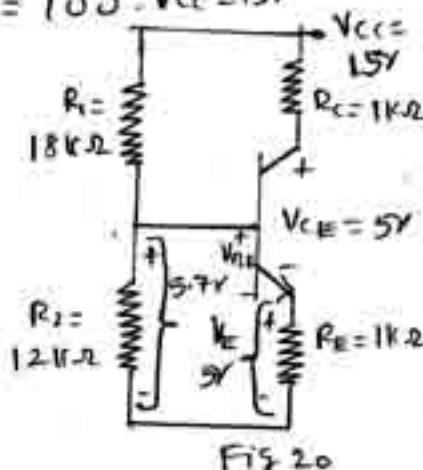


Fig 20

Step 4: $R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{15 - (V_{BE} + V_E)}{500 \times 10^{-6}} = \frac{15 - 0.7 - 5}{500 \times 10^{-6}} = \underline{\underline{18.6\text{k}\Omega}}$ (Use 12kΩ standard value)

Step 5: $R_c = \frac{V_{CC} - V_{CE} - V_E}{I_c} = \frac{15 - 5 - 5}{5 \times 10^{-3}} = \underline{\underline{1\text{k}\Omega}}$ (Standard value)

The Voltage divider bias circuit is shown in Fig 20

i) Design the Voltage-divider bias circuit to operate from a 12V supply. Given $V_{CE} = 3V$, $V_E = 5V$ & $I_C = 1mA$.

Given $V_{CC} = 12V$, $V_{CE} = 3V$, $V_E = 5V$, $I_C = 1mA$.

Assume $V_{BE} = 0.7V$.

Step 1: $I_2 = I_c = \frac{1 \times 10^{-3}}{10} = \underline{\underline{100\text{nA}}}$

Step 2: $R_E = \frac{V_E}{I_c} = \frac{5}{1 \times 10^{-3}} = \underline{\underline{5\text{k}\Omega}}$ (Use 4.7kΩ standard value)

Step 3: $R_2 = \frac{V_B}{I_2} = \frac{V_{BE} + V_E}{I_2} = \frac{0.7 + 5}{100 \times 10^{-6}} = \frac{0.7 + 4.7}{100 \times 10^{-6}} = \underline{\underline{57\text{k}\Omega}}$

$R_2 = \underline{\underline{57\text{k}\Omega}} \text{ } \textcircled{2} \text{ } \underline{\underline{54\text{k}\Omega}} \text{ (If } R_E = 4.7\text{k}\Omega)$

(Use 56kΩ standard value)

Step 4: $R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{V_{CC} - V_{BE} - V_E}{I_2} = \frac{12 - 0.7 - 5}{100 \times 10^{-6}} = \frac{12 - 0.7 - 4.7}{100 \times 10^{-6}} = \underline{\underline{12.0\text{ }\textcircled{2}\text{ }\frac{12-0.7-4.7}{96.4 \times 10^{-6}}}}$

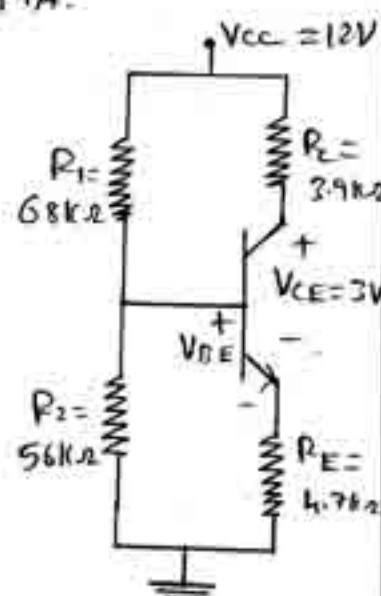


Fig 21

$$R_c = 63\text{ k}\Omega \text{ @ } \underline{\underline{68.46\text{ k}\Omega}}$$

Step 5: $R_c = \frac{V_{cc} - V_{CE} - V_E}{I_C}$

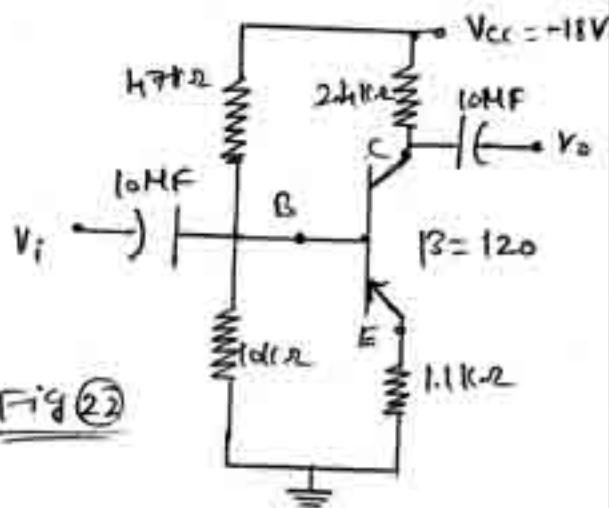
$$= \frac{12 - 3 - 5}{1 \times 10^{-3}} \text{ @ } \frac{12 - 3 - 4.7}{1 \times 10^{-3}}$$

$$R_c = 4\text{ k}\Omega \text{ @ } \underline{\underline{4.3\text{ k}\Omega}}$$

(Use $3.9\text{ k}\Omega$ standard value)

The Voltage-divider circuit is shown in fig(21)

- ② Determine V_{CE} for the
Voltage-divider bias
configuration of fig(22)

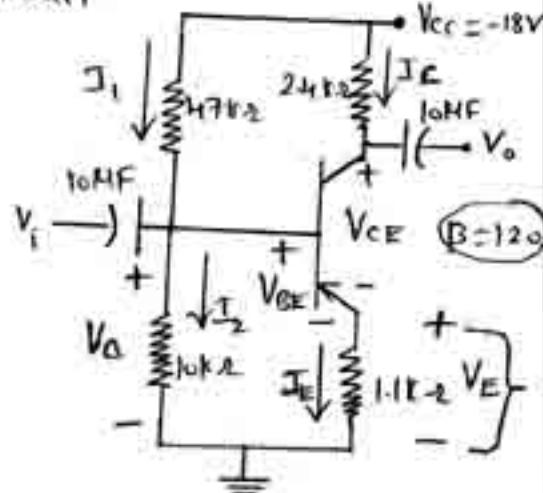


Fig(22)

- ③ The given Voltage-divider bias circuit
is shown in fig 22 @

$$V_B = \frac{-V_{cc} R_2}{R_1 + R_2} \quad \left[\begin{array}{l} -V_{cc} - I_1 R_1 - I_2 R_2 = 0 \\ @ \quad I_2 = -\frac{V_{cc}}{R_1 + R_2} \left(\frac{I_1}{I_2} \right) \\ V_B = \left(\frac{-V_{cc}}{R_1 + R_2} \right) R_2 \end{array} \right]$$

$$= \frac{-18 \times 10k}{47k + 10k} \text{ @ } 0.7 = -3.16V$$



$$V_E = V_B - V_{BE} \quad [\because V_B = V_{BE} + V_E]$$

$$= -3.16 - (-0.7) \quad \left(\begin{array}{l} V_{BE} = -0.7V \\ \text{for PNP transistor} \\ \text{with a bare circuit} \end{array} \right)$$

$$= \underline{\underline{-2.46V}}$$

$$I_E = \frac{V_E}{R_E} = \frac{-2.46}{1.1 \times 10^3} = -2.24 \text{ mA} //$$

$$I_C \approx I_E = -2.24 \text{ mA} //$$

$$V_{CE} = -V_{CC} - I_C(R_C + R_E) \quad [-V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0]$$

$$= -18 - (-2.24 \times 10^{-3})(2.4k + 1.1k)$$

$$= -10.16 \text{ V}$$

(Q) The given voltage-divider bias

$$I_2 = \frac{V_{CC}}{R_1 + R_2} = \frac{18}{4.7k + 1.1k} = 0.316 \text{ mA}$$

$$\because -V_{CC} + I_1 R_1 + I_2 R_2 = 0 \\ I_1 \approx I_2$$

$$V_B = I_2 R_2 = 3.16 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.16 - 0.7 = 2.46 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.46}{1.1 \times 10^3} = 2.24 \text{ mA}$$

$$I_C \approx I_E = 2.24 \text{ mA} //$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 18 - 2.24 \times 10^{-3}(2.4k + 1.1k)$$

$$= 10.16 \text{ V}$$

